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BEHAVIORAL ANALYSIS OF INSULATED GATE BIPOLAR TRANSISTORS DURING HARD AND SOFT TURN-OFF

BY

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B.S., Kettering University, 2006

THESIS

Submitted in partial fulfillment of the requirements
for the degree of Master of Science in Electrical and Computer Engineering
in the Graduate College of the
University of Illinois at Urbana-Champaign, 2007

Urbana, Illinois

Adviser:

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ABSTRACT

This thesis examines hard and soft turn-off behavior of insulated gate bipolar transistors. Insulated gate bipolar transistors are used as switching devices in power converters for machine drives. Faults during operation of converters occurring due to reasons such as loss of control, device parasitics, and load-side malfunctions might necessitate shutdown of the devices to protect them from destruction. Hard turn-off entails a direct shutdown when a fault is detected, whereas soft turn-off involves a relatively slower shutdown to prevent overvoltage stress and consequent breakdown of the device. For short-circuit conditions, soft turn-off helps reduce overvoltage. However, for overcurrent situations, several factors are evaluated to determine whether soft turn-off should be used: the amount of parasitic inductance, the turn-off overvoltage, and the capability of the power device to handle higher current for brief intervals. Also, soft turn-off uses excess pulse energy due to longer turn-off time. This excess energy leads to increased losses and potential to hurt the device. Thus, the trade-off is to maximize overvoltage reduction for the least increase in pulse area. Through simulations and hardware tests, it is shown that soft turn-off for short-circuit current is necessary but for overcurrent conditions, the decision whether to use hard or soft turn-off is application based.

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To my parents

ACKNOWLEDGMENTS

I would like to extend my gratitude to my adviser, Dr. Philip Krein, for offering excellent advice and timely suggestions for improvement in my work and constructive criticism during evaluations. Additionally, I would also like to thank my supervisor T. V. Sriram, at Delphi Electronics and Safety Systems in Kokomo, Indiana, not only for recommending me for the Delphi Scholarship to pursue graduate studies at the University of Illinois but also for his feedback and ideas during the hardware validation of the thesis. I would further like to thank the engineering and technology support staff at Delphi Advanced Powertrain and Power Electronics group for their input and suggestions; in particular, I thank Robert J. Campbell, Senior Power Semiconductors Specialist Engineer, for device physics and high-voltage printed circuit board layout related inputs.

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1. INTRODUCTION

1.1. Motivation

The desire to understand the behavior of insulated gate bipolar transistors (IGBTs) during soft turn-off is the motivation behind the thesis. IGBTs are used as switching devices in dc to dc converters and dc to ac inverters. To protect them from destruction during faults, which lead to high current, they are shut down in most cases as soon as the fault is detected. Shutdown is carried out in two ways: immediate (hard turn-off) or a relatively slow decrease of gate voltage (soft turn-off). The first method involves the risk of overvoltage breakdown of the device, whereas the second uses more power and hence dissipates more energy. This may thermally affect the device. Observing the behavior of different IGBT types during hard and soft turn-off after faults will help clarify the areas or applications where they could be incorporated.

1.2. Literature Review

Design of high performance gate drives and incorporation of protection circuitry within them has been the subject of extensive research. In [1], the requirements of a typical gate drive circuit are described, with a tilt towards physical properties of the IGBT. References [2-4] describe unique gate drive circuit designs with added protection circuitry. Circuit designs to optimize turn-off during short-circuit conditions are shown in [5]. Studies in this area have been geared towards high performance gate drive circuit designs. The use of additional components such as snubber circuits to achieve maximum performance has been discouraged [6]. Further,

innovative circuitry has been developed to incorporate sensing of faults and protection of the IGBT from them, and to ensure safe turn-off of the device should a condition forcing the same arise. Active driving and fault protection is discussed in [7-9], where the gate voltage is varied in several stages during switching, to optimize properties of the gate drive and also ensure protection and minimal losses.

IGBT structural differences and modeling challenges constitute an important portion of this thesis. IGBT structures and their salient differences are introduced in [10-13]. Modeling issues in IGBTs and techniques to account for nonlinearities in their behavior are mentioned in [14, 15]. This thesis examines the behavior of IGBT structures during turn-off after a fault. Hence, it is a useful addition to the ongoing research on innovative fault detection and protection circuit design.

1.3. Overview of Document

For better comprehension of the thesis, it is necessary to understand some background information regarding the use of IGBTs in inverters, classification of faults that can occur in machine drives, IGBT structures, different faults that arise during operation of converters which can affect the IGBT, and important features of gate drive and protection circuitry. In Chapter 2, the extensive use of IGBTs in dc to ac inverters is highlighted and faults are classified into two broad categories. In Chapter 3, readers are given a brief history of IGBTs and their innovative structures. Salient features of different IGBT structures are highlighted and categorized based on device physics and layout. Additionally, recent structural developments in IGBT technology are compared to previous versions. In Chapter 4, the phenomenon of desaturation experienced by IGBTs during overcurrent or short-circuit conditions is

introduced. The three ways an IGBT may fail in short-circuit conditions are described. Potential hazards of hard turn-off are highlighted. Requirements and general characteristic of gate drive circuits are introduced in Chapter 5. The necessity of protecting power semiconductor devices and the process of desaturation detection are also highlighted here. Simulations and hardware experiments follow in Chapters 6 and 7. Observations are reported in Chapter 8. The thesis concludes with recommendations on future work in Chapter 9.

2. FAULTS IN IGBT INVERTERS

To understand turn-off behavior of IGBTs, it is beneficial to have some background on the use of IGBTs in inverters and faults that can occur in them. In this chapter, the widespread use of IGBTs in dc to ac inverters is highlighted. Faults are classified into two broad categories and elaborated.

2.1. IGBTs in Inverters

Pulse-width modulated (PWM) inverters and other power conversion circuits use IGBTs because they are easily driven and have high current-carrying capability. Medium and high voltage dc to dc converters, as well as dc to ac inverters, use IGBTs or MOSFETs as switches playing an inherent role in their operation. Figure 1 shows an application where six IGBTs are used in the demonstrated configuration in a three-phase inverter. Three-phase inverters are ubiquitous components of machine drives. IGBTs are controlled through their gate. When a voltage higher than the threshold voltage of the device is applied across the gate and emitter, the IGBT turns on and begins to conduct current through the collector-emitter junctions.

A significant portion of losses in PWM power converters is due to switching of the semiconductor devices such as the IGBTs [16]. These losses can be classified into two types: dynamic and static losses. Dynamic losses occur during the switching process, i.e., the transition from a conducting to a nonconducting state and vice versa, owing to the overlap of nonzero voltage and current during this process. Static losses occur during conduction because of on-state resistance in the MOSFET and constant voltage drop in the IGBT [17].

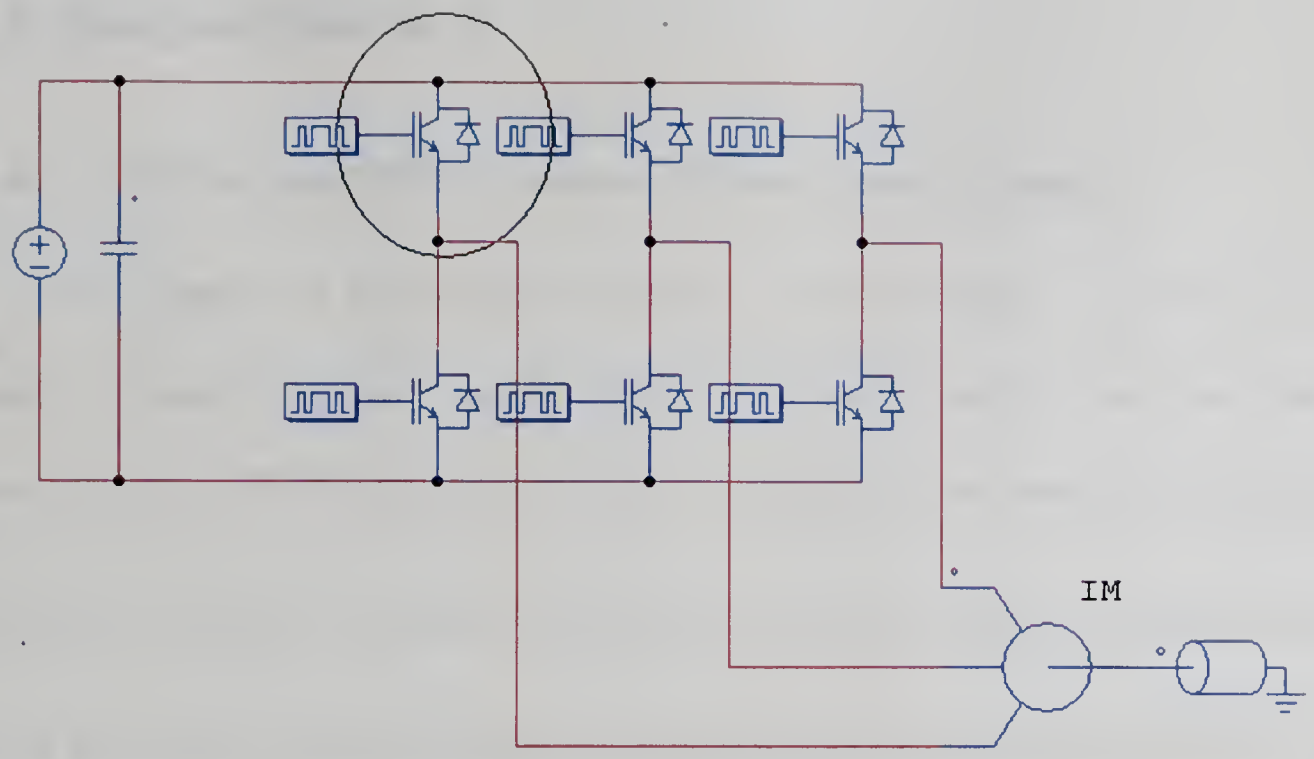


Figure 1: IGBT used as a switch in a three-phase inverter

In [18-20], the extensive use of switching functions to analyze inverter operations and losses is shown. Owing to conventional switching operations in inverters such as the PWM, the switches are exposed to variable frequencies as well as duty cycles. Hence, switch protection is necessary to ensure reliable operation of the system [21]. System requirements such as device stress versus low commutation losses demand conflicting designs of the gate drive.

2.2. Inverter-Driven Machine Drive Faults

Industrial as well as hybrid electric vehicle machine drives are subject to various faults. They can be broadly classified into hard switched faults and faults under load [22]. These are elaborated in the following subsections.

2.2.1. Hard-switched faults

2.2.1.1. Device parasitic components and shoot-through

An example of hard-switched faults is a shoot-through in an inverter leg. Parasitic turn-on of the lower device during the turn-off process of the upper device causes this event. The nonlinear gate-collector capacitor of the lower IGBT undergoes a $\frac{dv}{dt}$(rate of change of voltage) which results in a flow of current through it directly into the gate node, causing a voltage to develop across the gate-emitter junction. This developed voltage exceeds the threshold voltage and turns on the device. To avoid this, the gate is clamped to the low potential when not in conduction mode. Equation (1) describes the current that results in a capacitor due to a rate of change of voltage. The capacitor is a nonlinear function of the gate-collector and gate-emitter voltage.

$$i = c(v)\frac{dv}{dt} \tag{1}$$

2.2.1.2. Dead-time and shoot-through

Turn-off of the upper IGBT is not synchronous with turn-on of the lower. An error in control can result in overlap between turn-off of the upper IGBT and turn-on of the lower one. This can also cause shoot-through current, when the alternate IGBT in the same leg turns on while the upper IGBT is conducting. The turn-off of IGBTs is associated with tail current due to bipolar junction transistor (BJT) related current-carrying properties. This shoot-through effect is countered by adding asymmetry in terms of passive components or incorporating a turn-on time delay at the gate drive [23]. This time delay is known as dead time.

2.2.2. Faults under load

Faults under load are caused during conduction due to unforeseen and unfavorable changes in the load, such as ground faults and line-to-line faults. The former occurs when a phase line is accidentally connected to ground and the latter describes a sudden undesired connection between phase lines. They are shown using dotted lines in Figure 2. The converter side shows the shoot-through scenario, whereas the load side shows the line-ground and line-line faults.

When faults arise, the current flow through the power semiconductor devices rises, causing the device to overheat and rupture. Hence, it is beneficial to have integrated protection circuitry included within a gate drive that detects faults and consequently enables circuitry to protect the device by either reducing the gate voltage and thereby the collector-emitter current, or shutting off the device.

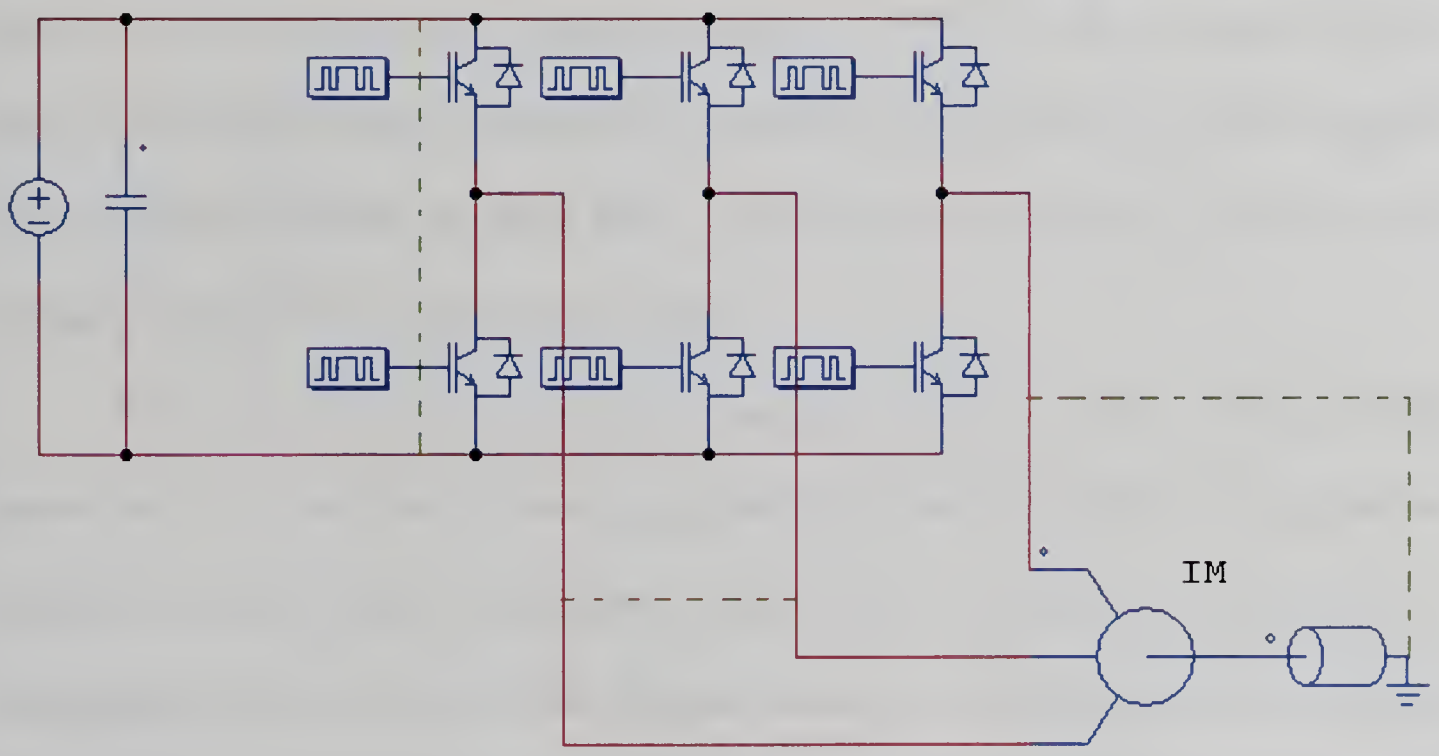


Figure 2: Faults in inverter-driven systems

3. OVERVIEW OF IGBT STRUCTURES

This chapter begins with a brief history of IGBT invention. The properties of different IGBT structures have been highlighted and further grouped into categories based on device physics and layout. The pros and cons of each structure with respect to conduction loss, switching loss, short-circuit ruggedness and ease in paralleling are discussed. Also, recent structural developments in IGBT technology and their superior properties as compared to predecessors have been mentioned.

3.1. History

The IGBT is conceived as a hybrid device of the power MOSFET and the BJT. The impetus behind its development was to obtain a switching device with high current-carrying capabilities that was easy to control. BJTs have high current-carrying capability due to their dual junction structure. MOSFETs are voltage-controlled devices with fixed on-state characteristics and high input impedance. These properties were coupled to create the basic IGBT, which can be behaviorally modeled as a voltage-controlled high-current source [24].

IGBTs have evolved rapidly as a category of devices used widely in high power and low to medium-frequency applications. Formerly, MOSFETs were used in medium and low-voltage applications, whereas BJTs were used for higher power design purposes. In the early 1980s, designers made an attempt to utilize the desirable properties of the MOSFET and the BJT in high power as well as high frequency applications. Table 1 lists some IGBT characteristics when compared to a BJT and a MOSFET.

IGBT applications directly define which structural properties are beneficial and which are a hindrance. As an example, IGBTs are easy to control and have high current capability. The limits lie in switching frequency, as MOSFETs with the same voltage and current rating are faster. It is seen from Table 1 that the favorable properties of the BJT and the MOSFET are taken advantage of while designing the IGBT. High current-carrying capability and low on-state losses are good properties of the BJT that the IGBT inherits. A wide safe operating area (SOA), high input impedance, and low drive power are some positive attributes that the IGBT takes from the MOSFET. However, limits on switching speed and operating frequency still exist. It is useful at this point to review some basic points regarding the differences in IGBT structures [25].

Table 1: IGBT characteristics compared to a BJT and a MOSFET [26]

Features	BJT	MOSFET	IGBT
Drive Method	Current	Voltage	Voltage
Drive Circuit	Complex	Simple	Simple
Input Impedance	Low	High	High
Drive Power	High	Low	Low
Switching Speed	Slow (μs)	Fast (ns)	Middle
Operating Frequency	Low (Less than 100 kHz)	Fast (Less than 1 MHz)	Middle
S.O.A.	Narrow	Wide	Wide
Saturation Voltage	Low	High	Low

3.2. Physical Structure

It is known that power semiconductors are fabricated by implantation of

doped silicon, and their physical properties are based on the doping concentration of the silicon. On the basis of structure, the IGBTs fall under punch-through and non-punch-through categories [27] described in the following subsections.

3.2.1. Punch-through IGBTs

A cross-sectional view of the punch-through (PT) IGBT is shown in Figure 3(a). A PT-IGBT contains an n^+-buffer layer between the p^+- substrate and n^--drift region. A PT-IGBT is so called because the extension of the depleted region "punches through" the buffer layer before breakdown of the applied electric field can occur. It is also called asymmetrical IGBT. Fabrication of PT devices is foundational on a thick p^+ substrate (300 μm). Two doping levels are created, n^- and n^+, the latter being the buffer. The buffer layer is doped with n-type material (usually arsenic or phosphorous) that provides an additional electron per atom to aid in conductivity. This n^+-buffer layer acts as a recombination accelerator, in the process speeding up the turn-off process by curtailing the tail-current. The substrate has high concentration of p-type ions (usually boron) to enhance positive charge like properties. The trade-off between high switching speed and low on-state voltage is adjusted by the thickness of the buffer layer. The thicker the layer, the greater the recombination speed of the carriers during turn-off. However, the on-state voltage is likely to be high. This makes the punch-through IGBT viable for higher switching frequency related applications. Also, the PT-IGBT has favorable latch-up characteristics because the current gain of the parasitic p-n-p BJT is controlled. The PT device on-state voltage is less temperature sensitive because the additional buffer layer allows the stored charge to increase with temperature.

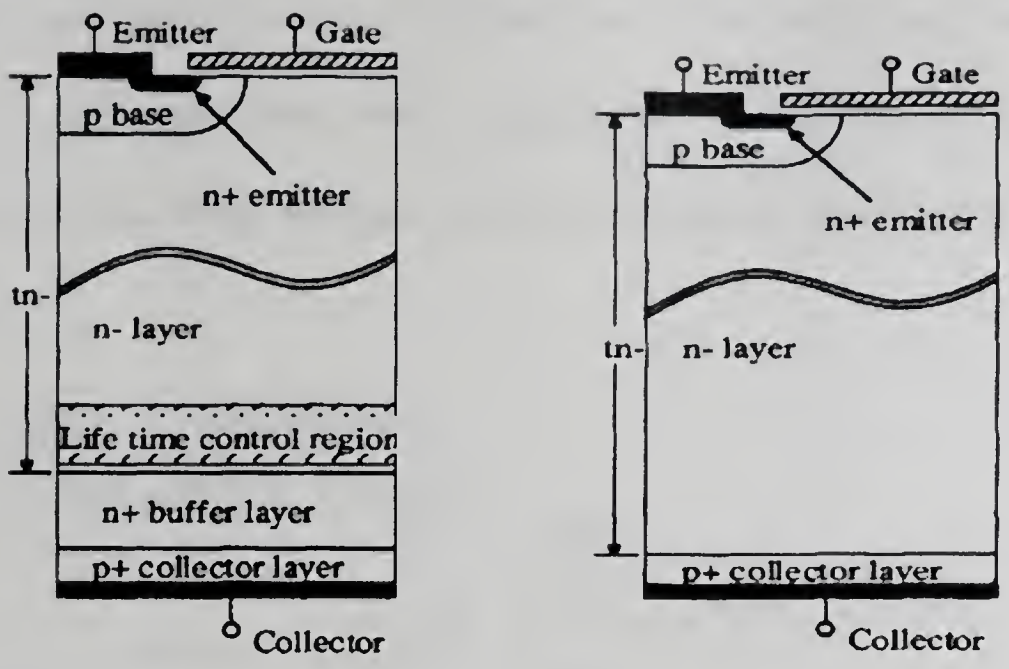


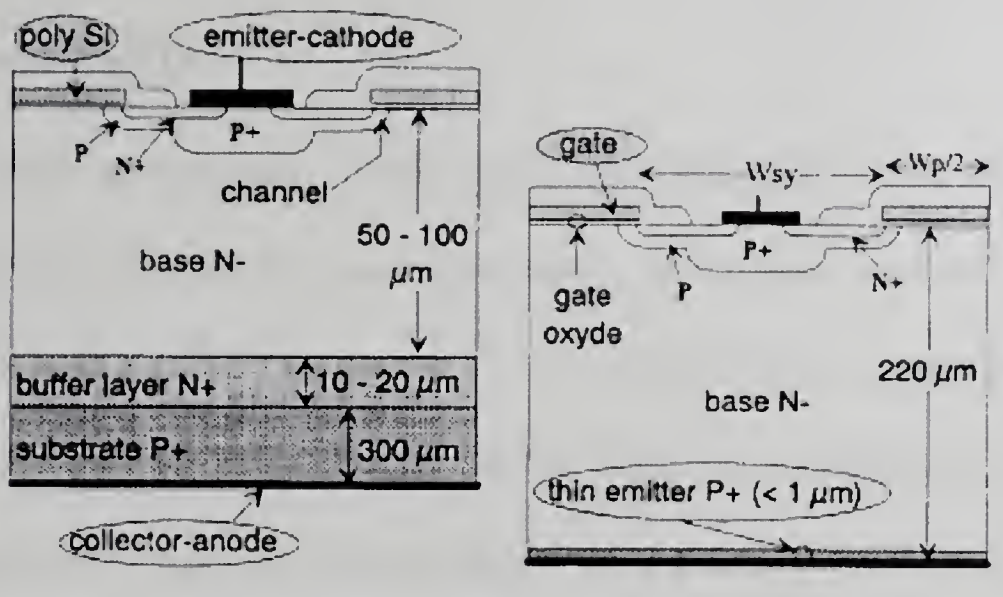
Figure 3: Physical structures of the (a) punch-through and (b) non-punch-through IGBT [12]

3.2.2. Non-punch-through IGBTs

The main difference between PT and non-punch-through (NPT) structures, as seen in Figure 3, is the presence of the n^+- buffer in the PT structure. Hence, NPT-IGBTs are thinner than PT-IGBTs, as shown in Figure 4. The total thickness of the NPT device is ~250 μm whereas that of PT-IGBT is almost twice as much. Hence, NPT-IGBTs dissipate heat more quickly and are thus a safer option for applications where short-circuit endurance is a necessity. Further, due to their wider base region and lower gain of the p-n-p BJT, NPT-IGBTs are rugged and short-circuit rated. This is the main advantage gained by trading off switching speed with NPT technology.

The structural ease of fabrication makes it desirable for NPT-IGBTs to be constructed at high breakdown voltages. The NPT technology's original substrate is the n^-layer [28]. This is the basic structure out of which the IGBT evolved and can be thought of as the concept initiator. Charge injection control is achieved in the base by adjusting the p^+-layer, which is diffused later in the process. The NPT-IGBT also

needs a thicker base region because of the absence of the buffer and overall thinner structure, which enhances short-circuit ruggedness. NPT-IGBTs are also overall suited for paralleling owing to their positive temperature coefficient of on-state voltage.



(a) (b)

Figure 4: Understanding relative thicknesses of (a) punch-through and (b) non-punch-through IGBT [29]

The PT on-state voltage value compared to the NPT counterpart is lesser. This difference is further enhanced at higher temperatures by the negative temperature coefficient of this property in PT-IGBTs. Turn-off switching loss for PT-IGBTs is hence also a factor of temperature, whereas NPT-IGBTs turn-off switching losses are nearly unaffected by temperature.

3.3. Layout-Based Approach

3.3.1. Planar IGBTs

The conventional structure of the power semiconductors is planar. Here, the conducting channel is horizontal, i.e., flow of current is horizontal across the device.

The gate polysilicon overlaps both channels to induce the electric field in order to begin conduction, as shown in Figure 5(a). Conduction losses are high in this structure because it has channel resistance R_{JFET} and $R_{Channel}$, which results in a higher on-state voltage.

3.3.2. Trench IGBTs

Reduction of conduction losses and higher integration were the motivations behind the development of the trench structure. The structure has a vertical channel. This is shown in Figure 5(b) where the horizontal length of the trench IGBT is much smaller and the channel exists around the implanted gate polysilicon. This ensures greater cell density since many more numbers of the IGBTs can be integrated into a unit of the same area.

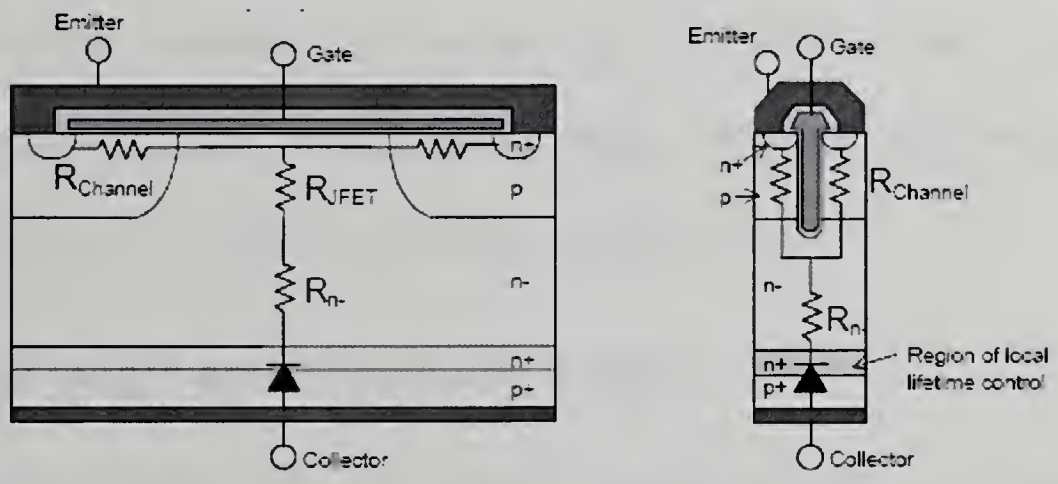


Figure 5: Layout-based classification of IGBTs: (a) planar and (b) trench structures [30]

When we compare Figure 5(a) and (b), it can be seen that around 4-5 trench cells can be included in the same region that the single planar cell occupies. This integration results in reduction of on-state channel resistance, elimination of the junction resistance, and greater channel width per unit area of the chip [31]. Additionally, robust turn-off properties are enhanced as a result of the modifications stated previously. Implantation of the polysilicon gate ensures complete inclusion of

the conducting channel around it, which further enhances uniformity in terms of electric field distribution. This enhances mobility of particles during dynamic behavioral stages.

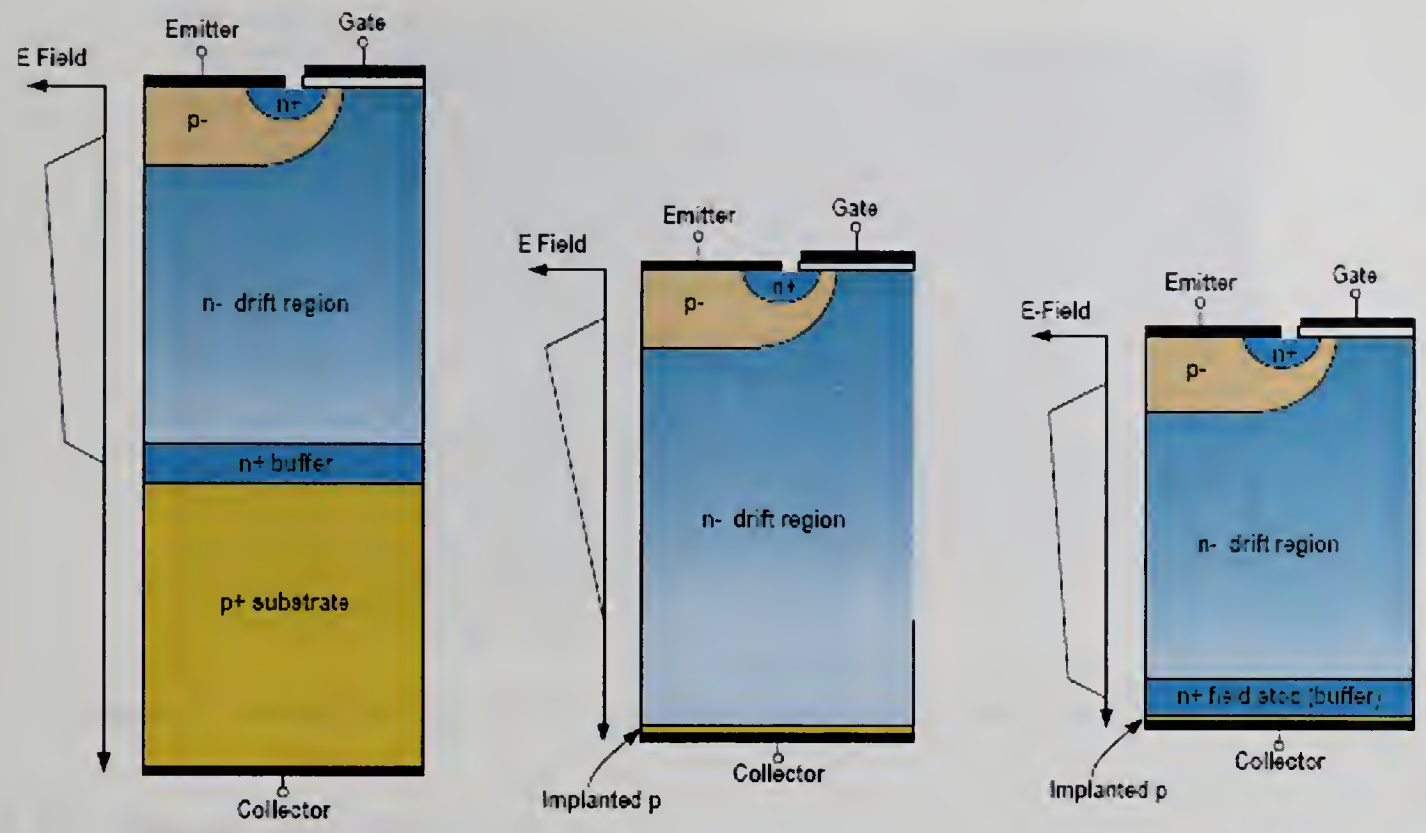
3.4. Contemporary Developments: The Field-Stop Structure

Conventionally, the light-punch-through (LPT) or the field-stop (FS) structure can be thought of as a subset of the NPT structure defined earlier. The NPT and PT IGBT are continuously improving technologies but still contain drawbacks. The former has a thick n^--base layer to enhance blocking condition. This causes higher static and dynamic losses than necessary. The latter has an unnecessarily high carrier concentration, resulting in high turn-off current and losses. For the same switching frequency, the NPT-IGBT has higher on-state voltage then the PT-IGBT. This difference is further enhanced by the fact that NPT-IGBTs have a positive temperature coefficient, i.e., their on-state voltage increases with temperature, whereas PT-IGBTs have a negative temperature coefficient [32].

3.4.1. Vertical length and trapezoidal E-field

An obvious improvement to the NPT structure would be to introduce a trapezoidal electric field distribution under the blocking condition. Hence, establishment of an FS layer with a low doping concentration that does not influence the p-emitter, but at the same time stops the electric field under blocking conditions, is desirable [33]. Reduction in vertical length of the NPT-IGBT is possible such that high blocking voltage properties are achieved when this layer is included. A typical vertical length of an FS-IGBT is 120 μm, as opposed to at least 175 μm for a NPT-

IGBT. This is evident in Figure 6. Also, the trapezoidal field coupled with the smaller structure combines the advantages of PT and NPT-IGBTs that make the FS-IGBT unique. The following paragraphs elucidate this statement.



(a) (b) (c)

Figure 6: Relative structural and electric field differences between the (a) punch-through (b) non-punch-through and (c) field-stop IGBT [32]

3.4.2. Switching speed and energy losses

The trapezoidal field of the FS-IGBT, also shown in Figure 6, expands as carriers are recombined and swept out during turn-off. This field terminates only in the field-stop n^+ region, thereby leaving almost no carriers left in the n^--drift region to recombine. As these carriers in the drift region are the major drivers of turn-off losses and tail current, FS-IGBTs, like PT-IGBTs, have a very short tail current (~0.3 μs) whereas NPT-IGBTs have the same for a few microseconds.

The conduction losses in FS-IGBTs are lower than NPT-IGBTs. The n^+ buffer region introduces the low on-state voltage properties of the PT-IGBT, thereby

keeping the losses low. From the above two statements, it is safely concluded that FS-IGBTs have lower losses than other counterparts (see Figure 7).

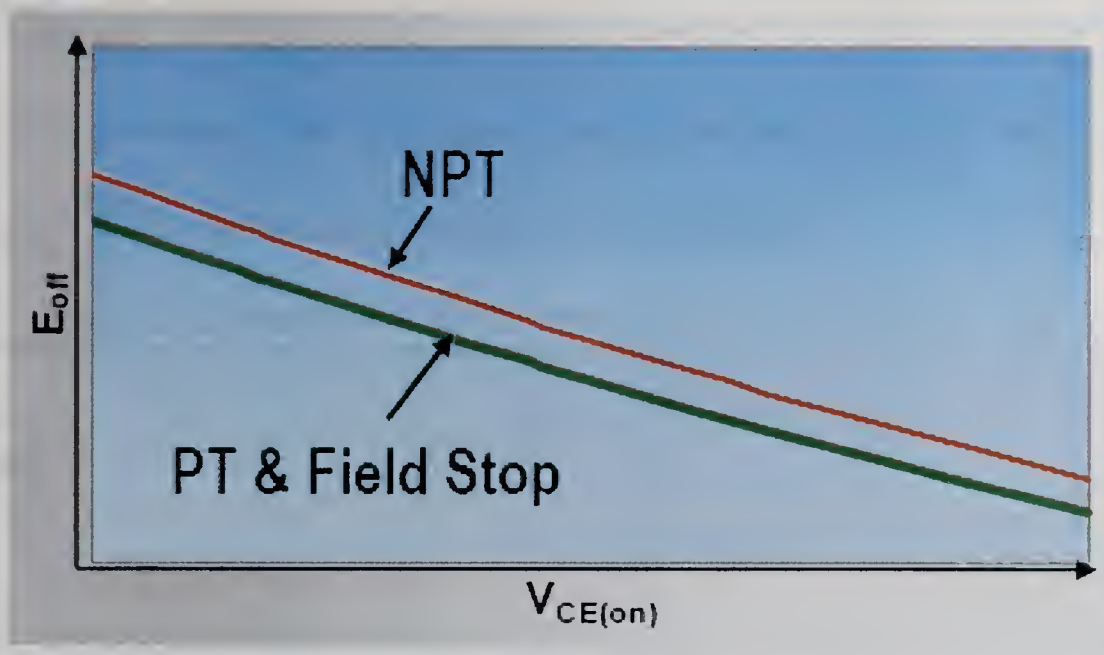


Figure 7: Turn-off energy Vs on-state voltage drop for different IGBT structures [32]

3.4.3. Short-circuit tolerance

It is natural to assume that when the FS structure is coupled with the trench arrangement, the resulting structure would be thinner and denser and have less current carrying capability. However, the smaller structure allows quick heat dissipation. Further, the trapezoidal electric field causes more homogeneous heat dissipation. Additionally, the well-known robustness of the NPT structure with the thick n-drift region remains unaltered. The combination of trench scale geometry, emitter efficiency, and carrier lifetime yields structures with short-circuit current tolerance up to five times the rated current for ~10 μs. This, when compared to the homogeneous distribution of heat made possible by the trapezoidal electric field, enhances short-circuit durability [34]. Hence, there is an expectation that the withstanding capability of short-circuit current by these field-stop trench devices will be greater [35], [36]. As

far as shutdown overvoltage capability is concerned, "thinner" structure would suggest worse breakdown characteristics. However, the n^--base layer is rugged and prevents this occurrence.

A summary of the discussed points is provided in Table 2, which shows that the FS-IGBT possesses the favorable properties and applications of both its predecessors. This is increasing its application possibilities.

Table 2: Comparison of IGBT structures and their properties [32]

	PT	NPT	Field Stop
Switching Loss	Low Short tail current Significant increase in E_{off} with temperature	Medium Long, low amplitude tail current Moderate increase in E_{off} with temperature	Low Short tail current Moderate increase in E_{off} with temperature
Conduction Loss	Low Flat to slight decrease with temperature	Medium Increases with temperature	Low Increases with temperature
Paralleling	Difficult Must sort on $V_{CE(on)}$ Must share heat	Easy Optional sorting Recommend share heat	Easy Optional sorting Recommend share heat
Short Circuit Rated	Limited High gain	Yes	Yes

3.4.4. Ease in paralleling

High-current applications often require IGBTs to be paralleled to enhance their current-carrying capability. During paralleling, appropriate sharing of current is necessary to avoid destruction of the IGBT due to current and hence thermal imbalance. Dynamic and static sharing issues need to be considered during design of IGBT parallel networks. Conventionally, device matching or sorting was carried out with respect to their properties such as threshold voltage and on-state voltage, before the IGBTs were paralleled. FS-IGBTs and NPT-IGBTs have a positive temperature

coefficient of on-state voltage and hence help reduce static and dynamic current flow during an imbalance. This enables self correction and, consequently, safe paralleling of IGBTs.

4. IGBT BEHAVIOR DURING FAULTS

This chapter distinguishes between overcurrent and short-circuit faults with respect to the current level. Also, the phenomenon of desaturation experienced by IGBTs during overcurrent or short-circuit conditions is introduced. Three ways that an IGBT may fail in short-circuit conditions are described. Finally, potential hazards of hard turn-off are highlighted. A note on short-circuit ruggedness and SOA of different IGBT structures is also mentioned.

4.1. Overcurrent and Short-Circuit Conditions

Load-side faults in induction machine drives exert high voltage and high current stress on the IGBT. An overcurrent condition, where the magnitude of the current flowing through the IGBT is typically 2-3 times the rated value, is likely to be temporary. A fault may also result in prolonged overcurrent or a short-circuit where the magnitude is at least 10 times the rated amount. The only factors limiting this rise in the circuit are the parasitic inductances, resistances, and the transconductance of the device, which has a negative temperature coefficient (decreases with temperature). Prompt detection of such a current rise in the IGBT and consequent protection are highly desired characteristics of gate drives [37].

4.1.1. Desaturation

Power semiconductors, when used as switches in energy processing power electronic circuits, are in their saturation stage. The on or off states of the device are predominant and care is taken in terms of gate drive design to ensure that there is very

little (ideally 0) time spent in the linear region. A fault condition causes high current flow when the device would ideally be in high voltage (off) state, or a voltage rise during on-state. In both cases, the result is simultaneous high current and high voltage in the IGBT, causing the device to shift from its saturation state to linear (amplifier) state, resulting in high power dissipation. This phenomenon is called *desaturation* [38]. Contemporary gate drives, such as the ones used in hardware validation (Chapter 6), contain desaturation detection circuits that sense this condition and activate protection circuitry that either temporarily reduces gate voltage to reduce current and avoid failure, or turns off the device altogether to prevent destruction.

4.2. Short-Circuit Failure Categories

The classification of short-circuits is based upon the manner in which they cause destruction of the device [39]. Figure 8 shows the three scenarios.

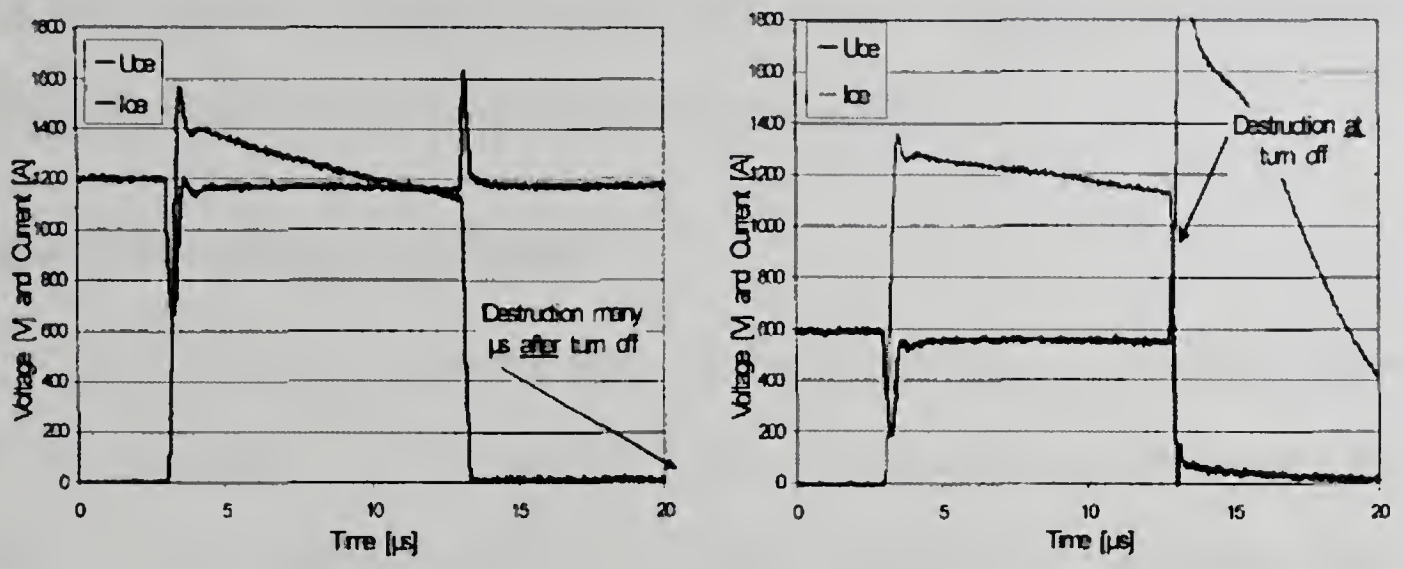
4.2.1. Thermal dissipation

In type I short-circuits, destruction of the IGBT occurs many microseconds after turn-off. This can be attributed to the failure in effective dissipation of heat, even after the protection algorithm is enabled and the device shut down. Generally, heat is simultaneously generated and dissipated by the IGBT. The power generated in the IGBT can be approximated as

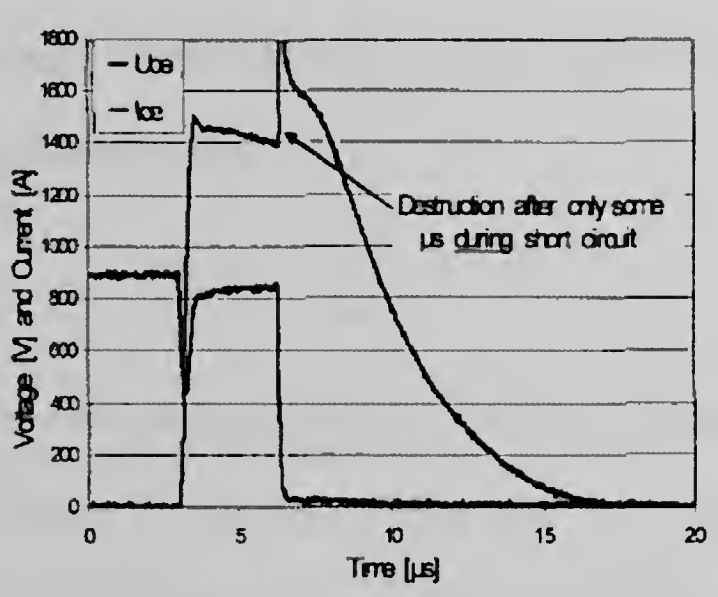
$$P_{gen} = \frac{T_j - T_a}{Z_{th}(t)} \tag{2}$$

In Equation (2), T_j and T_a are the junction and ambient temperatures of the device, respectively, and $Z_{th}(t)$ is the time-dependent thermal impedance. $Z_{th}(t)$ increases

with temperature until it reaches a steady state thermal resistance (R_{th}) value. The junction temperature needs to be maintained at less than some maximum temperature, as given by Equation (3).



(a) (b)



(c)

Figure 8: Types of short-circuits and their effects (a) type I, (b) type II, (c) type III [39]

$$T_j = Z_{th}(t)P_{gen} + T_a \leq T_{j\max} \tag{3}$$

Maintenance of junction temperature below the certain maximum value is possible only when the heat being dissipated is consistently more than the heat being generated. However, during short-circuit the current density in the device suddenly

increases. The heat generated in the device exponentially rises with current, whereas heat dissipated away from the device is a linear function of power generated. Thus, the heat rise during short-circuit is orders of magnitude higher than the dissipated heat. This causes the inability of the device to release the excess heat. Consequently, melting of the silicon occurs, causing device breakdown.

4.2.2. Overvoltage conditions

In type II short-circuits, the device is destroyed during turn-off. Likely causes are: (a) overvoltage occurring due to intrinsic inductances in the circuit, which if higher than the breakdown voltage, can destroy the silicon, or (b) latching, which occurs when the internal p-n-p-n thyristor of the IGBT latches at high current and high temperature, losing all control capabilities and hence becoming a self-amplifying current source, leading to destruction.

$$V_{overshoot} = L\frac{di}{dt} \tag{4}$$

Equation (4) describes overvoltage condition. This will be shown in simulation as well as the hardware results. During short-circuit hard turn-off, the rate of change of current is almost 10 times higher than normal. The package inductance is assumed to be constant. This causes a high overvoltage capable of destroying the device.

4.2.3. Latching

This phenomenon is best shown by referring to Figure 9. The IGBT has been shown to comprise discrete components: BJT and an n-MOSFET. When the gate is enabled and the device conducts, a sudden current surge causes the n-base (base of the n-p-n BJT) to take in high base current. In the process, it enhances conductivity of

the p-n-p BJT. This process continues as a cycle, as there is no external control over the conduction of the p-n-p BJT. Consequently, higher input current flows into the n-p-n BJT. Depending on the internal gain of the transistors, the current multiplies internally until the IGBT blows up.

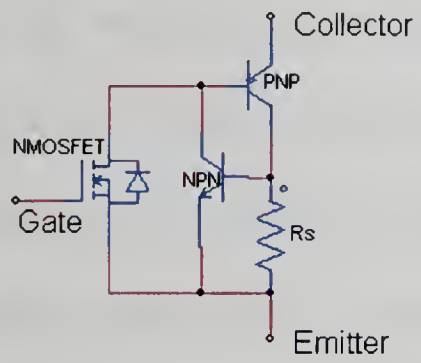


Figure 9: IGBT modeled with discrete components

Type III short-circuit is called *current destruction mode*. In this situation, the device is destroyed microseconds after the short-circuit condition begins. The likely cause is high current densities beyond the handling capability of the silicon, resulting in thermal shock which damages the crystal lattice and causes the temperature meltdown of the silicon.

4.3. Potential Hazards of Hard Shutdown

In the past, snubber circuits were used for overvoltage protection [40]. Soft turn-off through gate-side protection is an alternative to the snubber circuit, since this also can be integrated into the gate drive as opposed to using discrete components for the snubber circuit design. To protect the device from overcurrent, an overvoltage should not be induced. Hence, once a fault is detected, it is preferred to turn off the device "softly." In other words, instead of directly shutting off the device, the gate voltage is reduced gradually and then the device is shut off. This is done to protect it from any overvoltage stress that may occur during hard turn-off.

With soft turn-off, when an overcurrent is detected, the gate voltage is brought down gradually to limit the current, and then a turn-off is initiated. Hard turn-off is a straight turn-off of the gate once the overcurrent is detected. Soft turn-off includes increased turn-off time and the inability of the device being used again without a reset. It can be expected that for temporary overcurrent faults, the soft shutdown would not be incorporated, and thus normal operation would resume after a few microseconds once the gate voltage was brought down and current controlled.

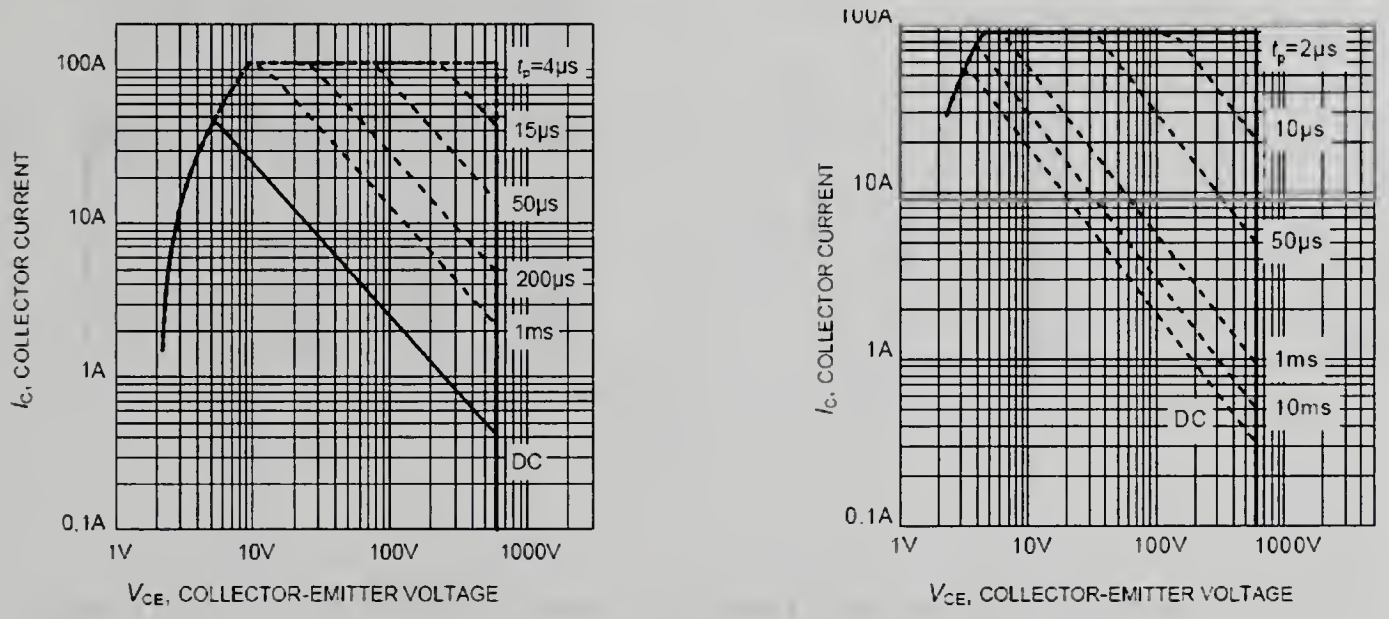
In soft turn-off situations, short-circuit is detected and the gate voltage is quickly reduced so that the short-circuit current is limited and then the turn-off initiated. Hence, soft turn-off helps protect the device from damage due to overvoltage.

4.3.1. Claim of trench technology

IGBT manufacturers and designers claim that since NPT trench structures are comparatively smaller and thinner than other structures (refer to Chapter 3), they have better heat dissipation capability such that soft turn-off is unnecessary [41]. The cost of the associated functionality and the losses due to extended turn-off could be avoided if soft turn-off was not incorporated. This is based solely on thermal breakdown. However, less silicon adversely affects the electrical breakdown characteristics, which are relevant in overvoltage related failures. A large part of the thesis will enhance the trade-off between electrical and thermal breakdown of the trench IGBT. The tests in the following chapters will show quantified evidence supporting or contradicting the claim.

4.4. Safe Operating Area and Short-Circuit Ruggedness

Safe operating area (SOA) is defined as the voltage and current conditions under which the device can be expected to operate without damage [42]. This section shows the SOA information of different IGBTs (Figures 10 and 11) that are used in hardware validation (Chapter 7). The IGBTs consist of one example each of the following: PT-planar, PT-trench, NPT-planar and FS-trench, all industrial TO-247 packages rated at 600 V (collector-emitter breakdown) and ~30 A (continuous). Infineon NPT-planar and FS-trench IGBTs has been used. International Rectifier PT-planar and PT-trench IGBT has been used. The maximum current allowed through each device for different pulse durations and collector-emitter voltages are shown.



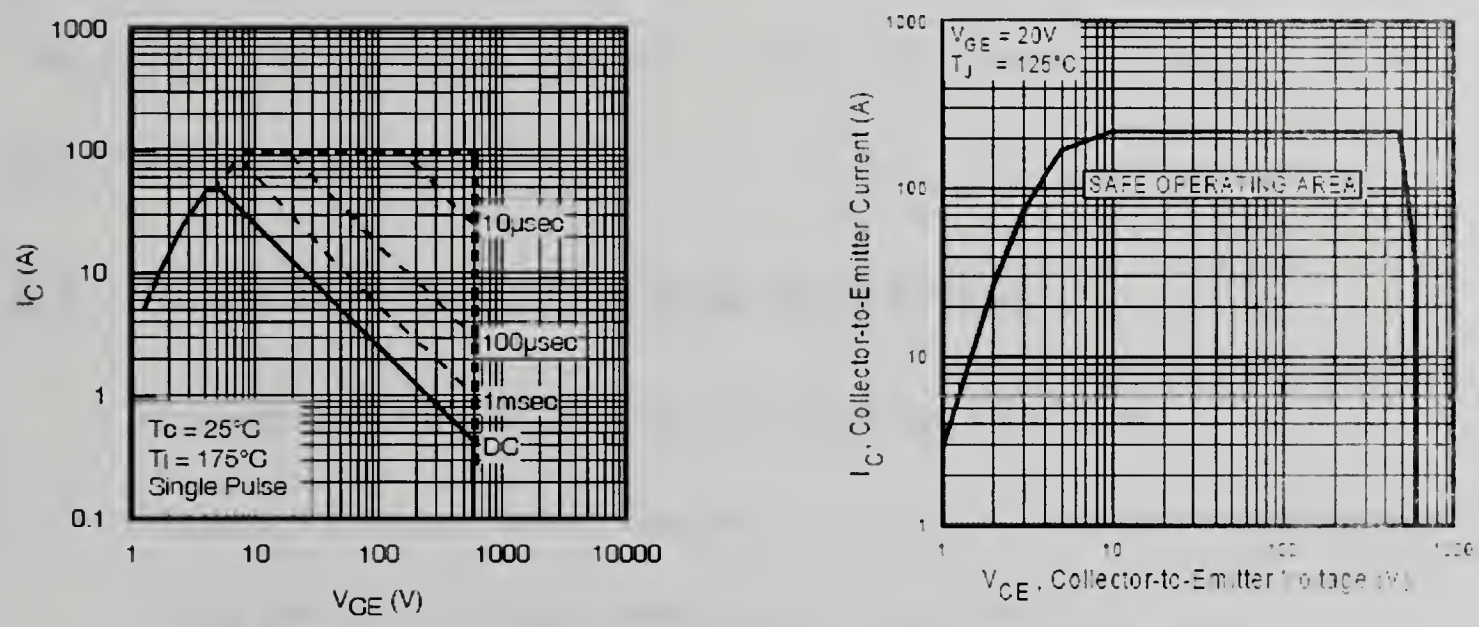
(a) (b)

Figure 10: SOA of (a) Infineon SKW30N60HS [43] planar and (b) Infineon IKW30N60T [44] trench IGBT

It is evident from Figure 10 that the NPT-planar as well as trench IGBTs are able to withstand around 100 A for about 4 µs. Further, Figure 11 shows that PT-planar IGBTs can carry up to 200 A for short durations (and trench IGBTs about 100 A for the same). However, does higher current carrying capability during short pulses

imply better short-circuit tolerance? This question is addressed during hardware validation, where higher short-circuit current (~200 A) is allowed to flow through the IGBT to see its turn-off behavior.

Switching trajectories in Chapter 7 give the voltages and currents the devices touch during experimentation. The validation shows that IGBTS withstand higher short-circuit current than the SOA limits suggest (see Section 8.4). The limits provided by the manufacturer are hence conservative as far as short-circuit tolerance information is concerned.



(a) (b)

Figure 11: SOA of (a) IRGB4062D trench [45] and (b) IRG4PC50UD2 planar [46] IGBT[1]

[1] Reference for part (b) only showed outer border of SOA, and not specific switching frequencies.

5. DRIVE AND PROTECTION CIRCUITRY

Designing optimized gate drives for IGBTs requires careful attention to application. As will be discussed in the following sections, gate drives need to be ideal in their specific applications, void of unnecessary attributes that add costs, and optimal in their trade-offs. Requirements and general characteristics of gate drive circuits with attention to physics of the device and its behavioral characteristics are introduced [40]. The necessity of protecting power semiconductor devices through the process of desaturation detection is highlighted. The idea of using the device gate-side circuitry for protection purposes is elaborated. The disadvantages of using current fuses are highlighted.

5.1. Characteristics of Optimal Gate Drives

Requirements of a gate drive can be summarized as follows:

- Mitigate switching losses: Designers incorporate minimum transition time during dynamic switching to mitigate switching losses.
- Reduce conduction losses during static stage: The device is fully enhanced (on) by applying 15 V or higher at the gate.
- Eliminate generation of harmonics due to high frequency oscillations during switching.
- Minimize voltage or current stress on the device during switching.
- Integrate voltage, current, and temperature sensors to control unexpected undesirable functioning.

- Achieve effective communication between drive and control circuit needed as a consequence of the above [47].
- Minimize transition time between logic "1" input and full enhancement of the device.
- Enable active clamping during off-state.

Simultaneous achievements of goals yield conflicting gate drive designs. To maximize application effects, trade-offs need to be made. Device properties and system-level performance requirements often have contrasting demands as far as gate drive design is concerned [8]. The value of the gate resistor is an example: a low gate resistor value increases switching speed due to the quicker charge of the gate-emitter capacitor but introduces high-frequency harmonics which are undesirable for system-level analysis. Increasing gate-emitter voltage for higher on-state enhancement also raises the chances of much higher overcurrents or short-circuit currents, should a fault occur.

Figure 12 shows an example of a gate drive with discrete devices. The level-shifter and the output stage are among the circuitry within an integrated driver chip. Apart from minimizing switching time and controlling dynamic effects, such as overshoots and reverse recovery during turn-on, the gate drive is also required to clamp the gate voltage after turn-off [9]. This is especially crucial in inverter-type applications where the devices are arranged in half-bridge legs. During turn-off of the upper device, the parasitic gate-collector capacitance of the lower device runs the risk of being charged, in the process undesirably turning on the gate [48]. An active Miller clamp, which is a feature in contemporary gate drives, is thus essential and ensures

reliability of the device and a nonconducting trait when the device is off. The algorithm pulls the gate down to the minimum voltage once a low voltage threshold level is reached during turn-off.

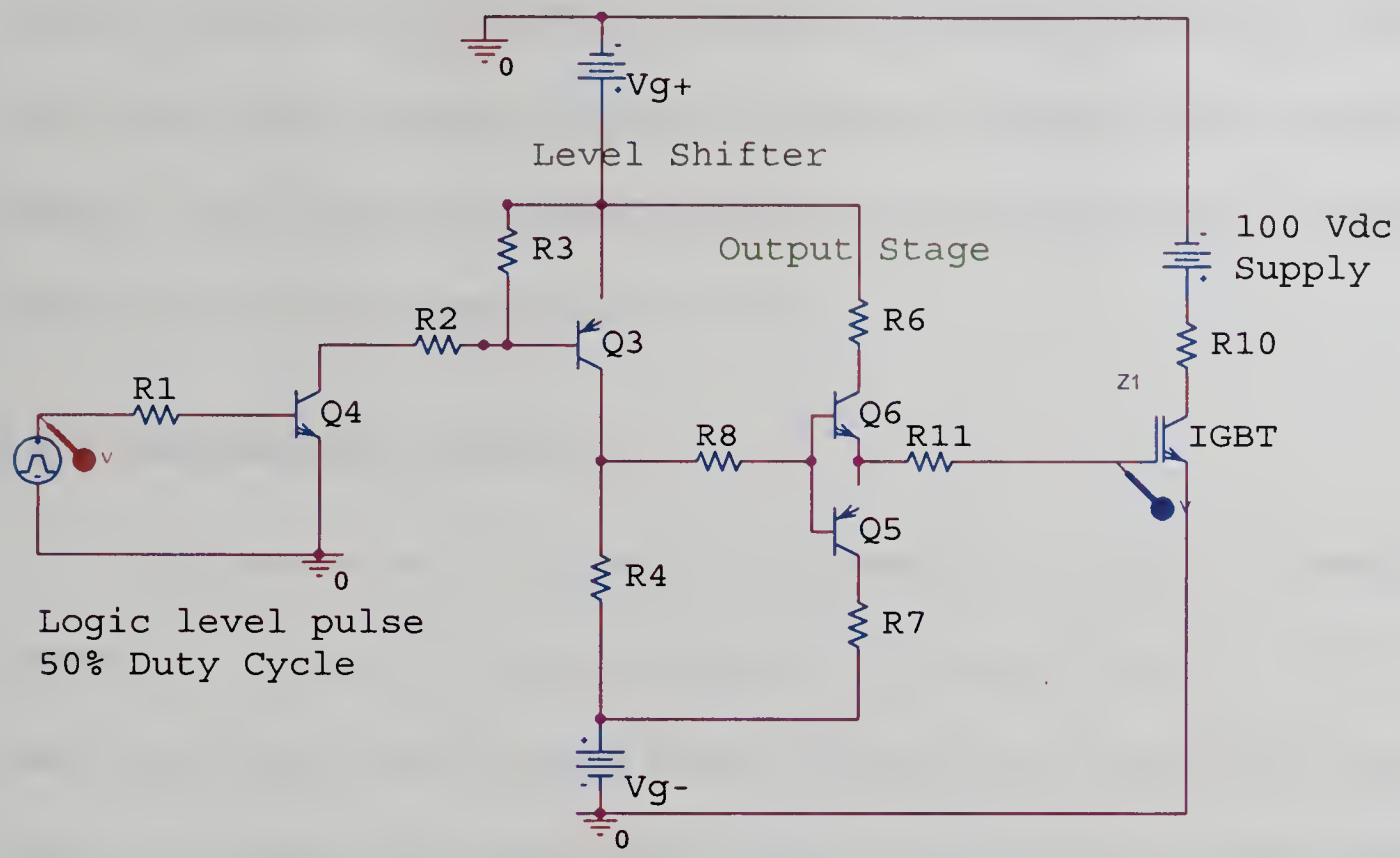


Figure 12: Example of a gate drive using discrete devices

5.2. Necessity of Protection

Broadly categorized, there can be three types of protection scenarios: protection due to voltage, current and parasitic elements. The defining examples for these, respectively, are: overvoltage, overcurrent, and parasitic turn-on. The protection circuitry is an additional feature that can be included in a gate drive. Depending on the application, electrical breakdown (overvoltage) or thermal breakdown (overcurrent) may be the likely cause of failure of the IGBT. While the former exists uniformly and is often mitigated by minimization of inductance in the layout, the latter is more specific to motor drive applications, where there is a high

likelihood of being switched into a fault or of having sudden low impedances due to undesirable changes in the load. Traditionally, snubber circuits have been used to counter overvoltage, whereas current sensors with feedback have been used to minimize overcurrent. Active Miller clamping avoids parasitic turn-on. Gate drives could employ local sensing techniques to combat overcurrent and overvoltage situations. These would avoid adding components in the circuit, thereby increasing losses and relative costs of production [49, 50].

5.2.1. Desaturation detection

The phenomenon of desaturation was discussed in Chapter 3. Detecting desaturation is one of the current techniques to protect IGBTs [51, 52]. The undervoltage lockout and desaturation protection algorithms are enabled after the gate signal is on. Undervoltage lockout keeps the gate shut off if the gate voltage is below a certain threshold value. The voltage at the collector node of the IGBT is sensed using a diode, and if it increases beyond a certain value (~8 V), the desaturation function is triggered. This initiates a turn-off of the IGBT. Further, depending on the functionality of the gate driver, the gate voltage is either taken to its minimum value instantaneously (hard turn-off) or the turn-off $\frac{di}{dt}$ is controlled (soft turn-off) to carry out a slow turn-off of the gate voltage. This takes longer but results in reduction of voltage overshoot [53-55].

An example circuit is shown in Figure 13. A gate driver with an optically isolated output stage is used to drive the IGBT. During regular on-state operation, the current through the opto-coupler turns on BJTs T_2 and T_3. Hence, the gate is pulled up

to high output-side voltage (V_{cc}). The diode D_1 is the desaturation-detecting diode. This diode is on during normal conduction but causes no interference with the operating circuit. The protection circuit is only active during the on-state of the device. This prevents unnecessary fault initiation during the off-state of the IGBT. During a voltage rise at the collector during conduction (desaturation condition) this diode turns off. The zener voltage is exceeded and thus the base current is allowed to flow through the zener D_2, turning on transistor T_1. This results in transistors T_2 and consequently T_3 turning off. Then, the only available path for the gate to discharge is through the resistor R_{GE}. This is because both n-p-n BJTs in the output stage are off (the lower because natural transition to off state was not made) and the diode in series with the gate node is reverse-biased. The timing between desaturation detection and shut-off of the IGBT is controlled to be below 10 μs, because contemporary IGBTs are typically rated to withstand short-circuit for up to 10 μs. The circuit shown in Figure 13 is hence an example of integrated desaturation protection in a gate driver.

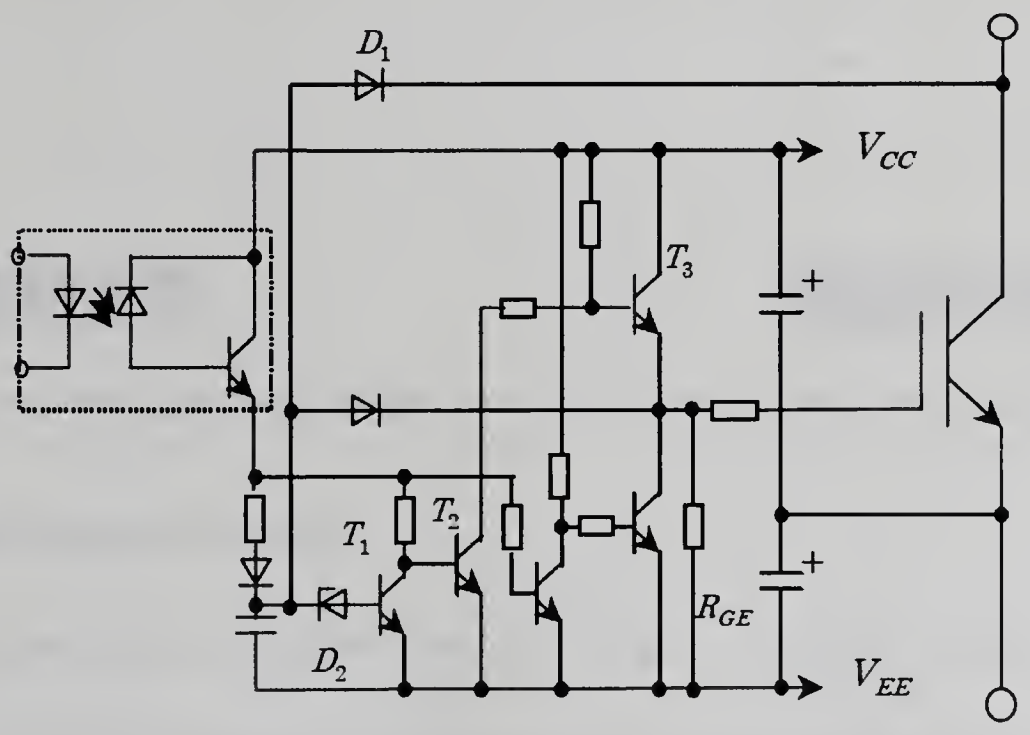


Figure 13: Desaturation detection circuit, within a gate driver [38]

To avoid unnecessary turn-off of the device due to noise, the desaturation detection circuit is not enabled until about 2-3 μs after the gate is enabled. This boosts accuracy as far as desaturation detection is concerned. Figure 14 shows this capability. Here the voltage at the desaturation pin is manually set to be 9 V. Only the drive stages are on and the power stage was off, since it is only a functionality test for the gate drive. The gate output voltage (Channel 1) is on for ~2.5 μs after turn-on and then shuts off after detecting 9 V (desaturation condition). The delay of 2-3 μs to allow settling of noise, and the validity of the gate driver are confirmed. The logic input (Channel 2) remains on while the driver shuts down on detecting desaturation.

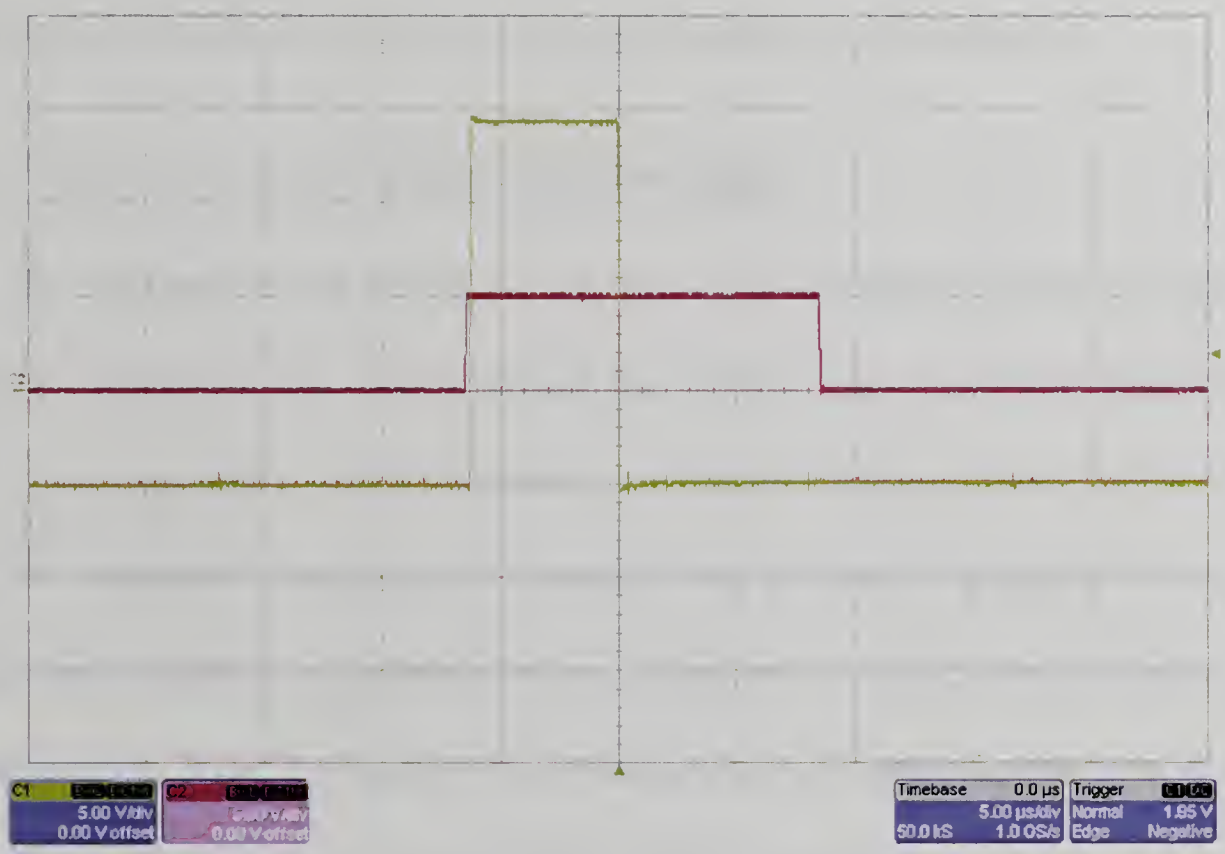


Figure 14: Gate drive output shuts off after detecting desaturation even while the logic input is on

5.2.2. Gate-side protection

The relative ease of control through the gate and already established control algorithms for GTO thyristors [56] prompted the idea of incorporating protection within the gate drive. Controlling the gate of the IGBT consists of charging and

discharging the gate-emitter and gate-collector capacitor, whose parallel combination is termed as the *input capacitance* [57]. Voltage or current sensors could be used to detect a fault in the circuit and trigger the protection circuitry. Consequently, contemporary gate drivers have the gate control block, protection block, and sensing block integrated into a single drive chip [58]. The low short-circuit tolerance time of the IGBTs further necessitates quick action, and consequently, the time between detection and shut-down of the device should be less than 10 μs. Monolithic integration of protection circuitry within the gate drive highly increases reaction time. Integrating several functions in gate drives also reduces the overall number of components in the circuit, thereby reducing the total cost of production.

5.2.3. Rated fuses and their disadvantage

A question can be posed on the use of a high-current fuse to rupture on detecting overcurrent and hence saving the device. This has three disadvantages. Firstly, fuses are bulky. Their inclusion in a circuit increases space and cost of an additional component. Secondly, the reaction time of fuses is typically in the tens of microseconds, highly undesirable when compared to short-circuit reaction time requirements in IGBTs. Finally, the reaction time of fuses increases with current rating. Hence, high-current applications would use fuses whose reaction time is more than a hundred microseconds. Considering that the short-circuit tolerance of IGBTs is less than 10 μs, they would be useless in these applications.

Fuses, with their connectors, are shown in Figure 15. They increase in size and hence current rating from left to right. The bulky size and higher reaction time due to materials used to build them, is apparent.

Figure 15: Plug-in type fuses used in various applications [59]

6. SIMULATIONS

This chapter describes simulations carried out to predict power losses and behavior of IGBTs under overcurrent and short-circuit conditions. The simulations are an exercise to view the desaturation effect and to estimate the upper level power loss in the pulse. Test procedures and schematic have been included. Graphs showing gate voltages, collector current, and collector-emitter voltage are shown. A discussion of the challenges of modeling IGBTs in simulators is also included.

6.1. Test Procedure and Objective

The objective of the simulation was to observe the desaturation process in an IGBT under high voltage and high current stress. A -5-V/15-V pulse was excited across the gate-emitter junction for 15 μs and the device was exposed to the worst case scenario with a small inductor to limit $\frac{di}{dt}$ during the overcurrent test and no inductive load during short-circuit test. For short-circuit simulations, the inductor was replaced by a short-circuit connection. The gate pulse, collector-emitter voltage, and collector-emitter current were plotted during the analysis. The IGBT model in the schematic will be explained in section 6.3.

6.2. Schematic

The schematic for overcurrent simulation is shown in Figure 16. A 10-μH inductive load was used during overcurrent testing. For short-circuit tests, the inductor was removed and replaced by a direct connection.

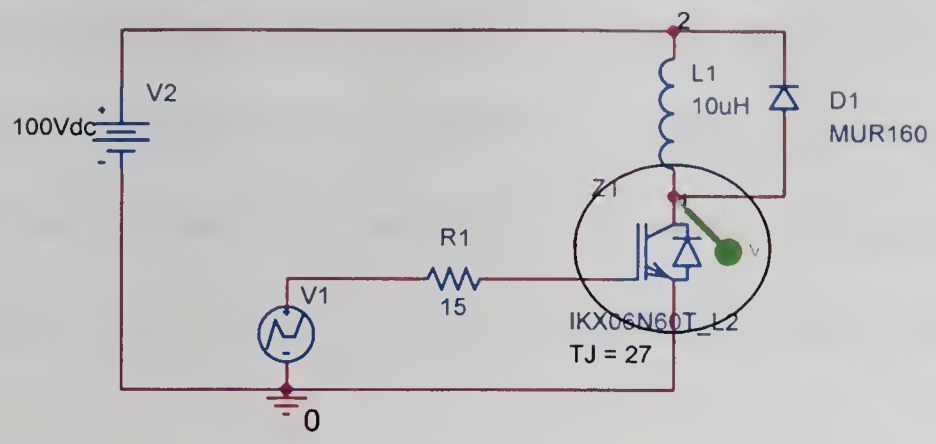


Figure 16: Schematic for PSPICE simulation

A 100-V dc supply across the IGBT is shown. A pulse generator V1 connects the gate of the IGBT through a resistor R1. The pulse generator was internally adjusted to provide a 15-μs pulse from -5 V to 15 V across the gate-emitter notes. The passive components causing parasitic effects are included within the model of the IGBT and hence are not visible in the schematic. An ultrafast recovery diode (MUR160) [60] was connected antiparallel to the inductor for freewheeling effect.

6.3. Optimized PSPICE Models

In Chapter 3, some salient features of the IGBT structures were identified. Internal structures of an IGBT show nonlinear phenomena. Examples of those features are: wide but lightly doped base region—which does not have a counterpart discrete BJT for representation, the ambipolar transport equation that describes the dynamic conducting behavior of the IGBT and nonlinear variation of gate capacitance with charge and gate voltage. Modeling a device with internal characteristics describing nonlinear phenomena requires not only discrete combination of already existing discrete devices and passive components, but also analog behavioral modeling (ABM) with controlled voltage and current sources [14, 15]. The limitations of simulators are another concern. Often, a trade-off needs to be made

between simulation time and dynamic accuracy. This is true particularly in case of switching devices in power electronic converters. Complex device physics, if added, complicate the simulation and increase the time. However, allowing higher levels of tolerance may often result in loss of accuracy, especially in the dynamic (switching) stages.

The PSPICE[2] models of the IGBTs tested were obtained from the web sites of their respective manufacturers (International Rectifier Corporation for punch-through and Infineon Technologies Incorporated for non-punch-through IGBTs) [61, 62]. PSPICE uses a hybrid class of models that incorporate both ABM and device physics to reach an optimum combination yielding accurate results in quick time. For purposes of this study, as mentioned, a 15-μs burst was used, and the time was not a factor. Hence, the default convergence settings were not changed, and a nearly accurate result was obtained.

6.4. Simulation Scenarios and Inferences

Figures 17 and 18 show desaturation in the IGBT when a single pulse is triggered across it. This would provide an upper level estimation of the energy dissipated in the pulse. Desaturation activates where shown. Consequently, the detection mechanism is also supposed to activate and shutdown the device. The power dissipation pulse was also monitored to calculate energy loss during the pulse. Equation (5) shows a sample calculation of the energy under a pulse during overcurrent condition. The power obtained is the product of the voltage and the

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[2] PSPICE is a product of Cadence Design Systems.

current across and through the pulse, respectively, and the energy is obtained by integrating the power across the on-time.

$$E_{pulse} = \int_{t}^{T} Pdt = 5.5\,\text{kW} * \Delta\text{T} = 5.5\,\text{kW} * 8\,\mu\text{s} = 44\,\text{mJ (approx.)} \quad (5)$$

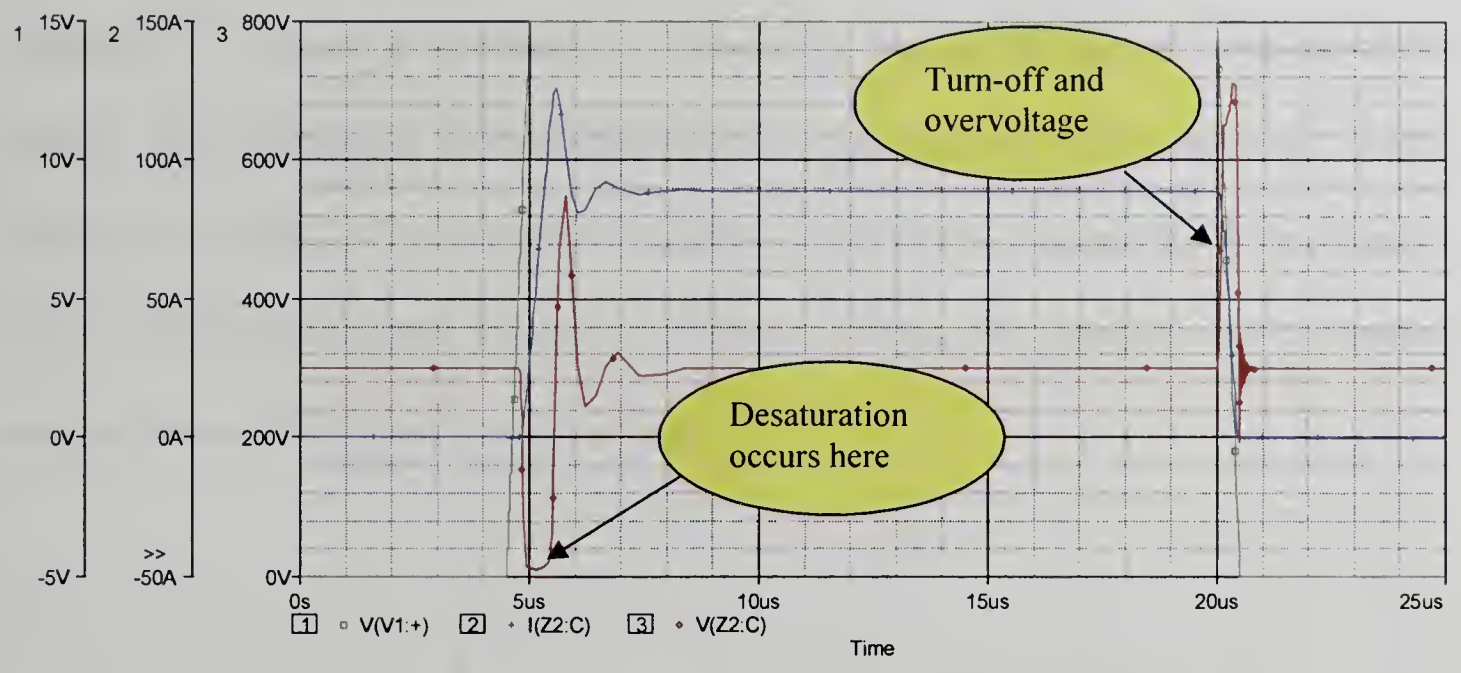

Figure 17: Simulation result during short condition: gate pulse, V_{ce} and I_{ce} are shown; time window is from 0 to 25 µs

Figure 17 demonstrates a short-circuit condition. When the gate pulse (Probe 1) is enhanced, the IGBT is in short-circuit mode and a high voltage (Probe 3) and high current (Probe 2) condition prevails. The only current-limiting factor is the temperature coefficient of resistance (depending on IGBT structure) and the transconductance limit, a result of reduction of gain in the IGBT with increase in temperature, as mentioned earlier. In the simulation, however, parasitic values of resistance and inductance were added to bridge the gap between reality and the ideal scenario. The voltage overshoot during turn-off is also shown to be almost double the dc bus voltage. This needs to be mitigated with soft turn-off. The IGBT model attempted to show short-circuit conditions effectively. However, the reducing value of transconductance at higher temperature was not portrayed accurately.

Consequently, an effective short-circuit current limit was not observed.

Figure 18 shows the results of the overcurrent simulation. The desaturation condition activates after the initial rise in the inductor current. Here, the collector-emitter voltage (Probe 1) begins to rise under high current. The protection circuitry discussed in Chapter 5 is expected to detect the rise in voltage and shut down the device. The simulation shows attainment of desaturation, and consequent higher current in the IGBT. The protection circuitry is supposed to initiate at the desaturation point. This will be validated in the next chapter. Further, the comparison of controlled and hard turn-off will also be carried out.

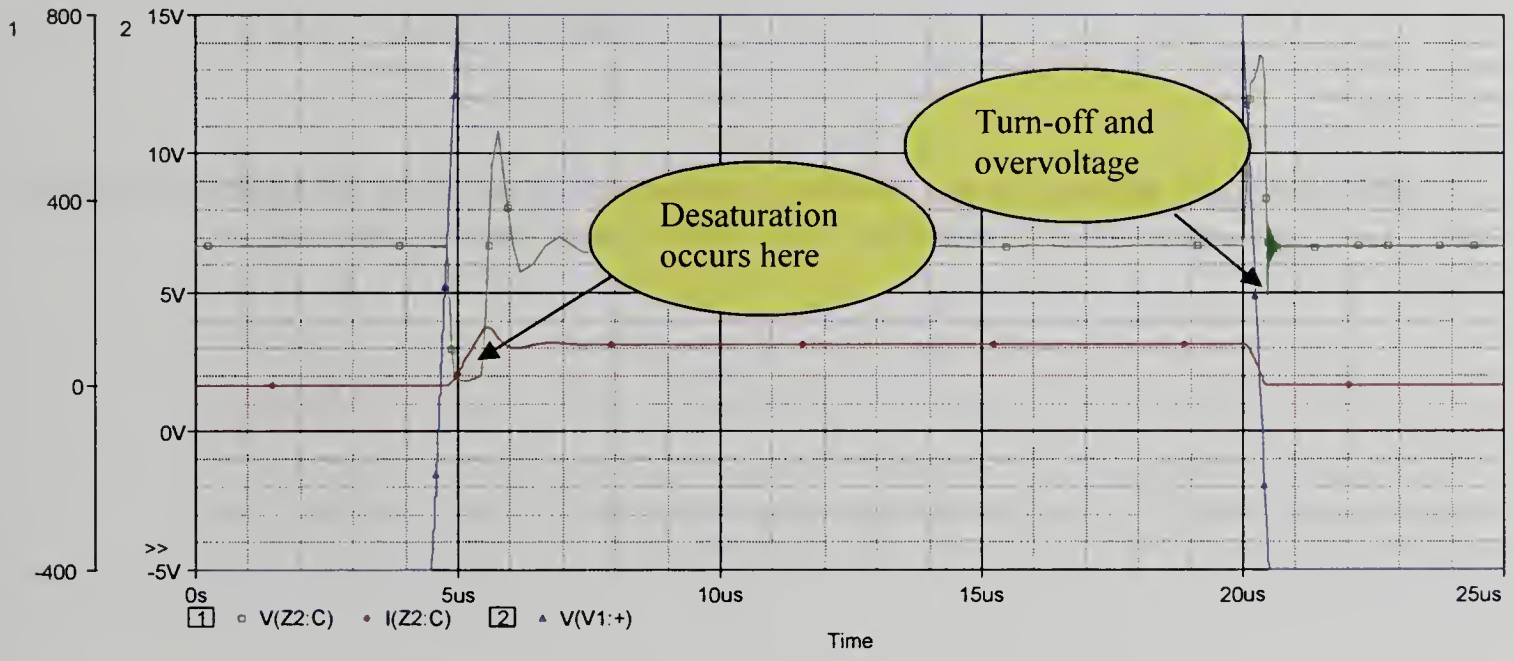

Figure 18: Simulation result during overcurrent condition: gate pulse, V_{ce} and I_{ce} are shown; time window is from 0 to 25 µs

An additional attempt was made to simulate short-circuit conditions, but this time without any parasitic components. Confirming the reasons for the initial assumptions, Figure 19 shows no change in voltage but a high current flow through the device when the gate pulse turns on; no dynamics are visible.

Thus, hardware was set up to validate the simulation results and also compare behavior of the IGBTs during hard and soft turn-off. The description is in Chapter 7. The equipment used for hardware validation is listed in Appendix D.

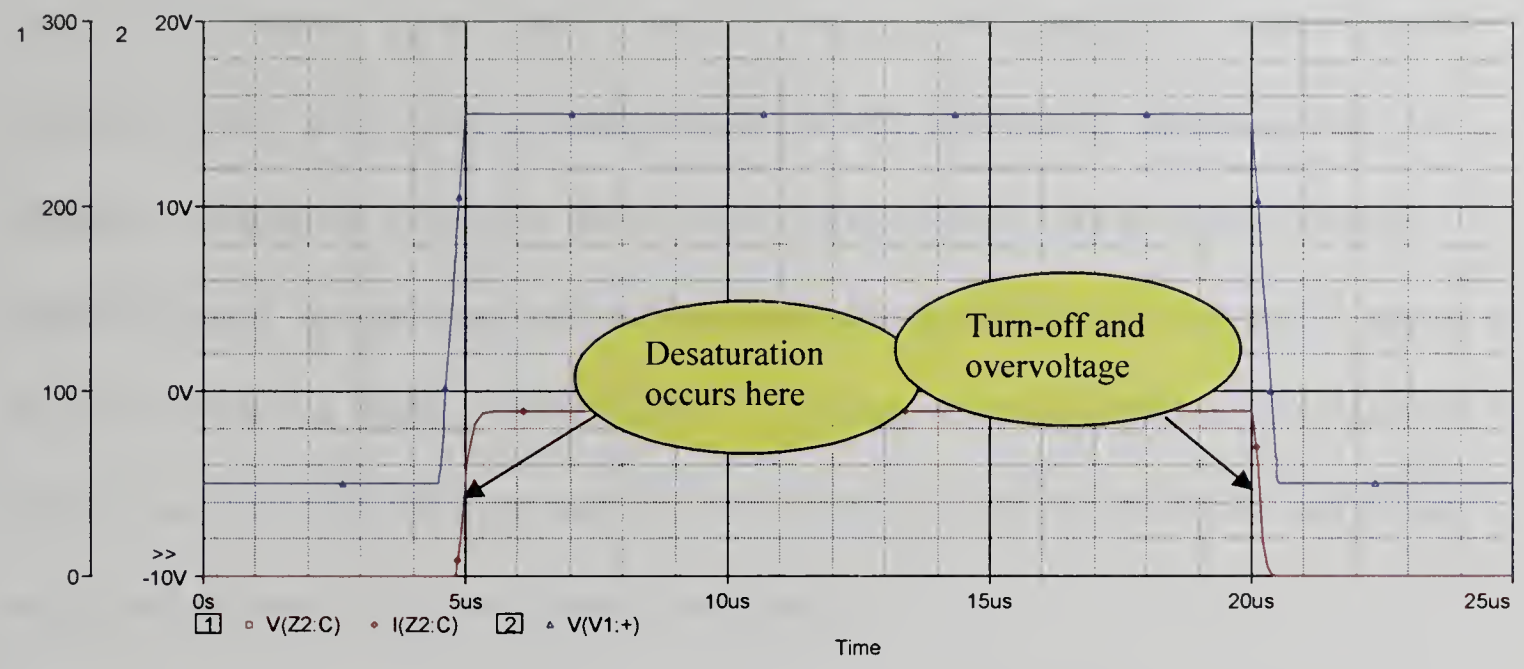

Figure 19: Simulation result during short-circuit condition and no parasitic component added: gate pulse, V_{ce} and I_{ce} are shown; time window is from 0 to 25 μs

7. TEST HARDWARE SETUP

This chapter provides details of the hardware experimentation. Schematics, layouts, challenges, and results are included. The set-up consisted of the gate driver and related circuitry on the drive side. The device under test (DUT) and a current viewing shunt resistor were connected in series with the load in the power stage. To maintain uniformity, an upper IGBT whose gate-emitter junction was shorted to ensure off state, was also connected. This upper device, which was a co-pack,[3] served as a free-wheeling diode. Various IGBT types and structures were tested. Snubber circuits were intentionally not included in order to expose the device to worst-case individual stresses in terms of current and voltage.

7.1. Overcurrent and Short-Circuit Test Setup Schematics

Figure 20 shows the circuit for overcurrent testing. The 1.56-μH load inductor is in series with the IGBT and the 10-mΩ current viewing resistor. The details of the gate drive with in-built protection schematic are shown in Appendix A. This gate drive initiates a pulse across the gate-emitter nodes to turn on the IGBT. Since the inductor is the only $\frac{di}{dt}$ limiter in this situation, overloading occurs in the circuit during the time the gate pulse is enabled. The current-viewing resistor is in series with the emitter. The pulse is manually triggered to turn on the device. The effect of the high current and high voltage transition with overloading conditions on the device can be seen.

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[3] IGBT with an antiparallel diode in a single package.

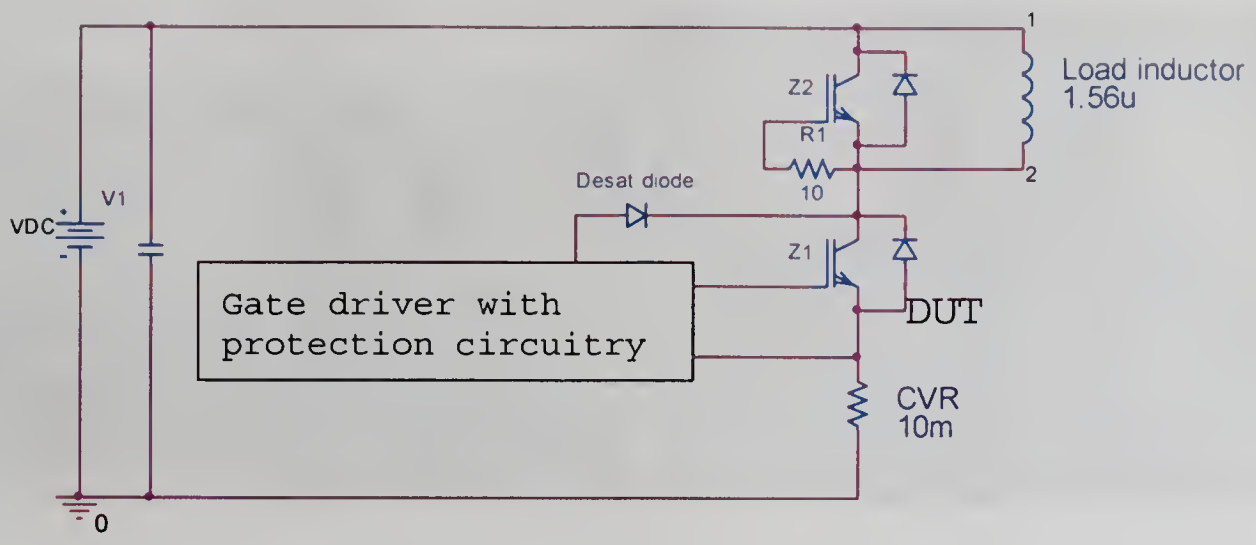


Figure 20: Overcurrent test schematic

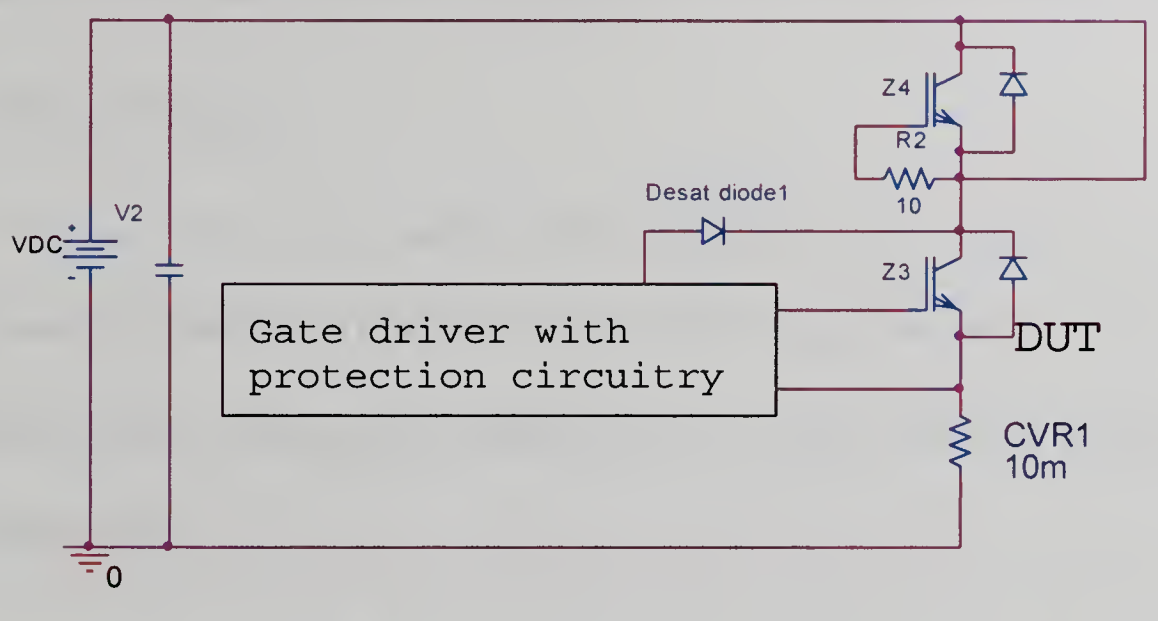
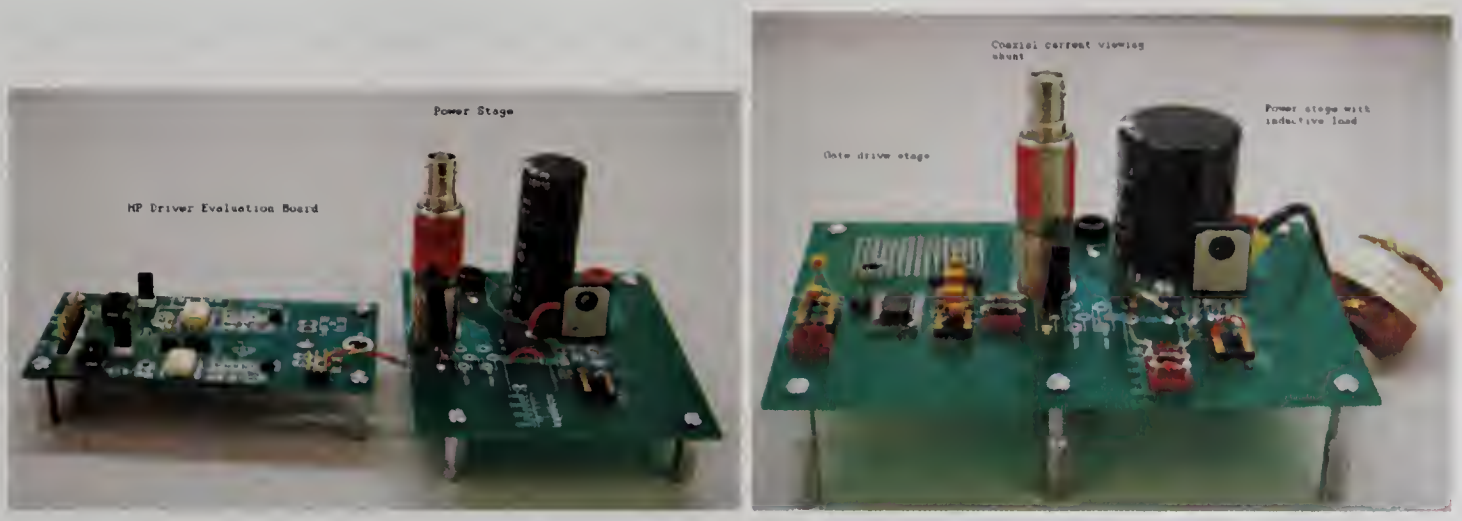


Figure 21: Short-circuit test schematic

Figure 21 shows the circuit for short-circuit testing. The inductive load was removed and the connection was shorted to allow the highest possible current and expose the device to worst cases. The only current limiters were the parasitic elements (resistances and inductances) in the circuit, and the transconductance of the IGBT. The transconductance has a negative temperature coefficient, which limited the gain of the IGBT and caused the current to flatten to a limit after the initial rise. Figure 22 shows the two setups. The major components of the setup are discussed in Section 7.2.



(a) (b)

Figure 22: Test setup for (a) HP evaluation board and (b) Infineon driver power stage[4]

7.2. Gate Driver

Two gate drivers were used for the hard and the soft turn-off, respectively. The Infineon EiceDRIVER 1ED020I12 single IGBT driver was used for hard turn-off applications whereas the Avago Technologies HCPL-316J was used to analyze soft turn-off applications.

7.2.1. Two-level turn-off

Two-level turn-off was a property promised by the Infineon 1ED020I12 single IGBT driver, as an added feature [63]. The soft turn-off process in this driver would be a two-step process. An external zener-capacitor parallel combination (see Figure 23) is added to the gate drive circuit to enable the function. The zener voltage is the median voltage stage to where the gate drive is initially brought. The capacitor, along with an internal resistor, decides how long the gate remains in this voltage before it is completely shut off. Due to unavailability of this function in the Infineon driver, it

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[4] The bulk capacitors shown were later replaced by 850 μF/450 V electrolytic capacitors for uniformity and better DC input voltage regulation.

was used solely as a hard turn-off driver, whereas the HCPL-316 J was used for soft turn-off.

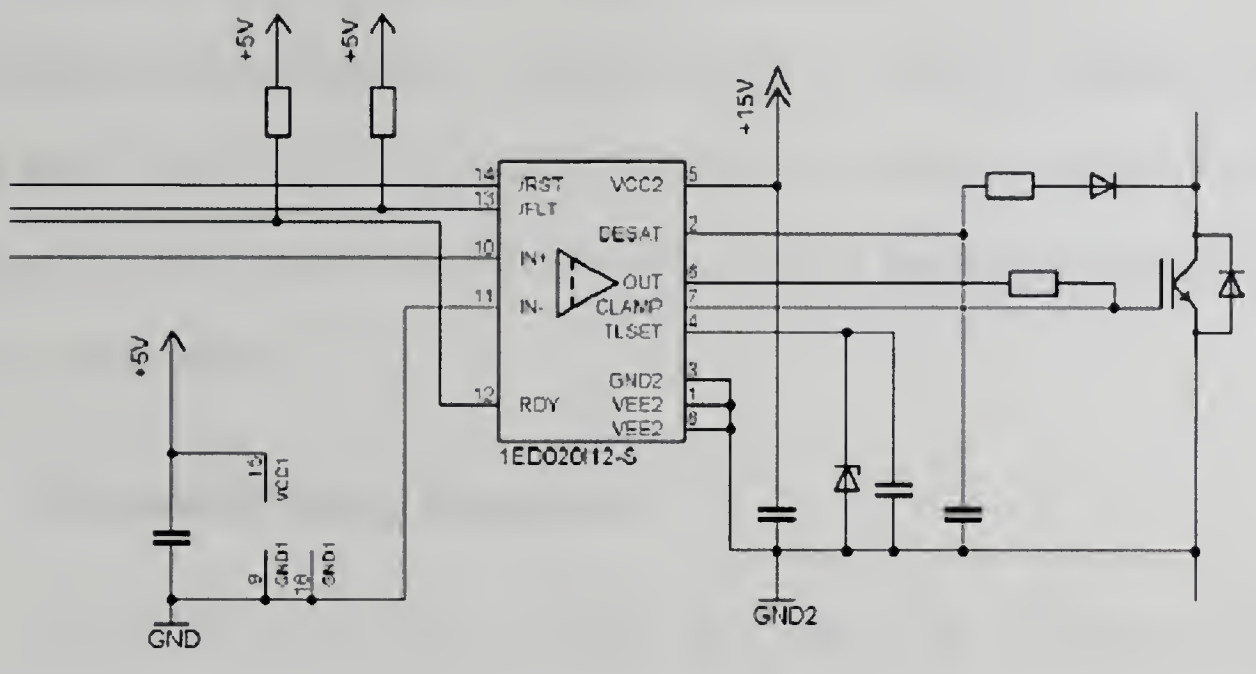


Figure 23: Infineon 1ED020I12 IGBT driver with application example [63]

7.3. The IGBTs to be Tested

Both NPT-IGBT and PT-IGBT structures under planar and trench layouts were tested. The packages were industrial TO-247 co-packs with built in ultrafast freewheeling diodes. A brief description of the IGBTs selected is provided as follows:

- SKW30N60HS: This is a high speed NPT-IGBT with a planar structure produced by Infineon Technologies. Rated at 600 V and 30 A continuous, it was available as a TO-247 package with a built-in freewheeling diode.
- IKW30N60T: This is a fast FS-IGBT with trench structure produced by Infineon Technologies and with ratings at 600 V and 30 A continuous.
- IRGP4062D: This is a 600-V TO-247 24-A continuous current trench IGBT manufactured by International Rectifier Corporation.

- IRG4PC50UD2: This is a PT-IGBT with a planar structure produced by International Rectifier Corporation. Rated at 27 A continuous and 600 V breakdown, it is also available in lead-free packages.

The collector-emitter breakdown voltage was 600 V, and the continuous current rating was ~30 A (27-31 A) to maintain consistency in silicon amounts. The other components were: 1.56-μH load inductor, 450-V/850-μF bus capacitor, and a 10-mΩ current viewing resistor.

7.4. Current-Viewing Resistors

Current-viewing resistors (CVRs) are rugged high frequency resistors designed to sustain the very high peak power and current inputs generated by capacitor banks, pulse generator systems, and steady state current loads [62]. Inherent in CVR design is a coupling between the major electrical parameters of resistance, bandpass, energy capacity, and wattage rating. *Pulse energy capacity* of a CVR is defined as the integral of the square of the peak current times the resistor value. Thus, the pulse energy capacity is the maximum recommended energy that should be dissipated in the CVR over a period short enough that losses are negligible. Most CVRs are designed primarily for surge current measurements; their rugged construction and low temperature coefficient resistive elements have made them ideally suited to a number of steady-state applications. An average wattage rating applicable to continuous current loading is thus quoted for each resistor series.

Shown in Figure 24 is a layout of the CVR used in the experiment. The S-end was inserted in the PCB and established a connection between the two layers, the emitter end of the IGBT to the floating ground (see Appendix A for detailed

schematic). The BNC-output is connected to the oscilloscope for direct current measurement. By "direct," the author implies that no sensors or transformers are used to estimate the current.

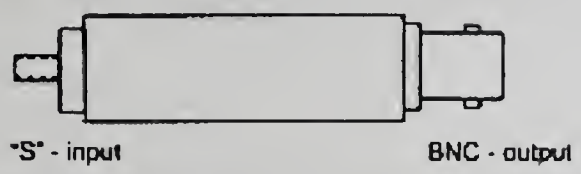


Figure 24: Series 'A' current viewing resistor used in validation [62]

7.5. Challenges in Hardware Development

Two-level turn-off functionality was not obtained due to manufacturing-related delay by the vendors. Hence, the HP driver, along with its evaluation board (see Figure 25), was used to obtain comparisons. However, owing to different manufacturing standards and product types, there was a distinct dissimilarity that caused initial discrepancy in the validation. The output stages of the two gate drivers were different. The Infineon driver had a totem-pole MOSFET configuration, and the HP driver had a triple Darlington configuration to increase the output current. This had two implications: the output charging current in the HP driver was larger than the Infineon driver but the output voltage across the gate-emitter was lower. The inherent diodes in the Darlington transistors would have a forward voltage drop of ~0.5 V, which would add up to cause this reduction in output voltage drop.

The above-mentioned discrepancy had to be accounted for since the drivers needed to be used simultaneously, and the difference between the amount of current in both overcurrent and short-circuit cases was desired to be around the first order of magnitude. Thus, the output stage power supply was manually increased during the

use of the HCPL-316 J driver so that the actual voltages across the gate emitter nodes were equal. Additionally, it is necessary to mention that no current buffer circuitry was added for two reasons:

- The device did not need more gate current than what the drivers were providing.
- Adding the buffer would negate any soft turn-off functionality, since the turn-off was no longer controlled by the driver.

Figure 25: Evaluation board for the HCPL-316J [64]

7.5.1. PCB layout and discussions

In this section, minimization of inductance during PCB layout is discussed. Package inductances (see Figure 26) and temperature are the two limiting factors in the current rating of an IGBT. Package inductances are a dynamic limiting factor owing to overshoot voltage during turn off. From Equation (4) earlier, V is the overshoot voltage that rises due to huge changes in the current level during turn-off and the inductances of the package. Out of this the stray inductance is a variable that can be minimized with good design tactics. This will enable the user to push the

limits of the current rating of the device [65].

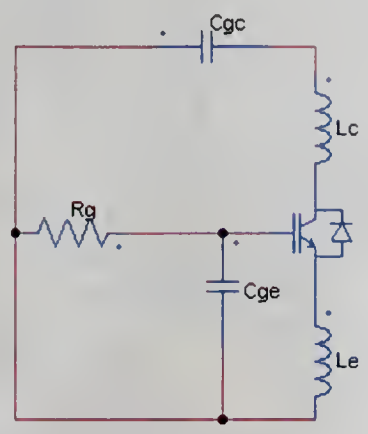


Figure 26: Inductances and capacitances internal to an IGBT

Shown in Figure 27 is the layout of the Infineon driver testing phase. To minimize inductance, large traces were used in the power stage that was carrying hundreds of amperes during the on-stage. Hence, there is a conspicuous difference in the trace sizes between the drive and the power stage. Also, the current shunt was mounted vertically on the PCB, and the current-sensing transformer was eliminated due to the sufficient accuracy of the shunt and addition of needless inductance. The PCB was initially designed to include the capacitor on board. Hence, the circular trace shows it. A bigger capacitor (450 V/ 850 μF) was used and connected in parallel to the input dc voltage. Also, numerous auxiliary holes (bottom right) were included in the PCB layout to account for any unforeseen changes in the schematic or new components that needed to be added into the circuit. The rectangular area of the auxiliary solder holes is also visible in Figure 27. Standard hole configurations for TO-247 device packages were used. Although only one TO-247 was needed, space was available for three. Extra holes allowed for changes which might arise because of ruptured device or displaced metal contact.

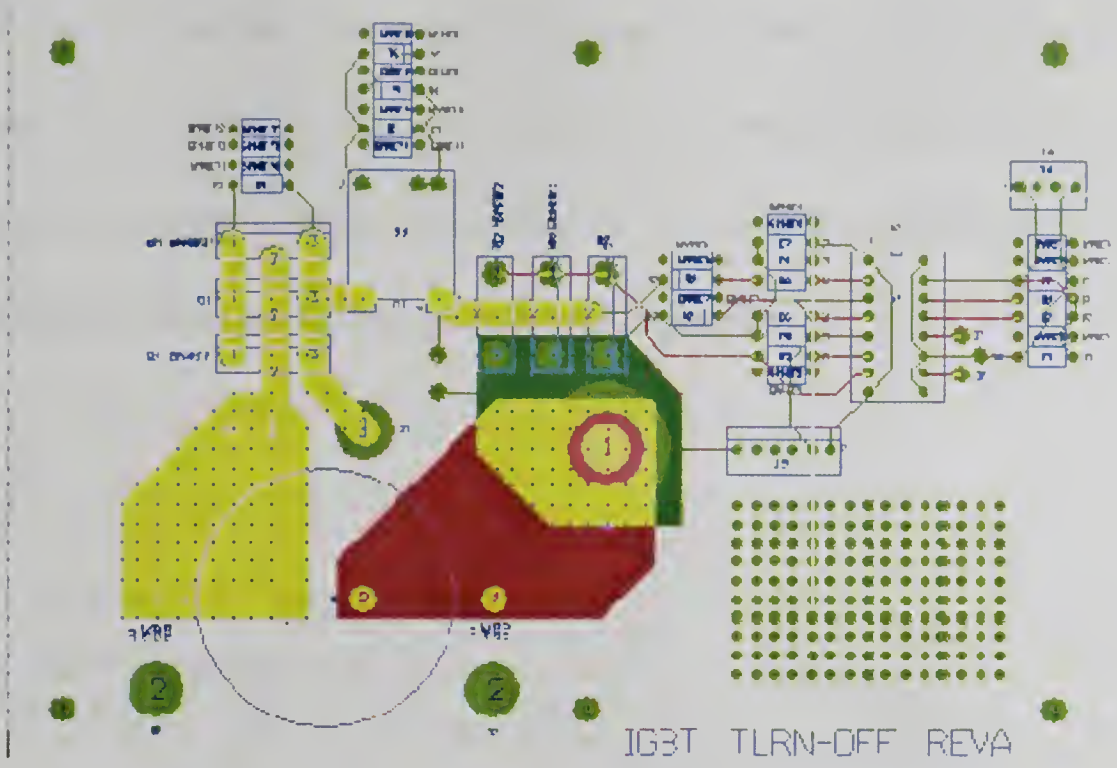


Figure 27: Layout of the Infineon driver testing phase

To save time, the evaluation board of the HCPL driver was connected to the power stage to test the IGBTs. The HCPL-316J evaluation board had a single-phase half-bridge driver configuration (see Figure 28 for schematic). The upper driver was disabled and the lower one was used. The schematic shown in Figure 28 includes the IGBTs, and details of the components used during the tests. For hardware test purposes, the IGBTs were externally connected. The gate and emitter of the IGBT were connected manually via wires to the lower output of the driver evaluation board. Care had to be taken to minimize inductance loops by shortening the wire length to ~1 inch and twisting the return path with the positive path to reduce area of loops. The only additional components to be included were the power supplies (logic, gate drive output, and high power) and the components in the power stage (IGBTs, CVR, and inductive load). The logic power supply is common for both drivers but the gate drive output power supplies were connected individually to each driver. Taking

advantage of this situation, the upper driver was disabled by not supplying gate drive output power. The HCPL-316J driver did not have the capability of disabling the soft turn-off to carry out any comparison. Hence, it was used to test soft turn-off behavior, a function that it would provide as an inherent capability.

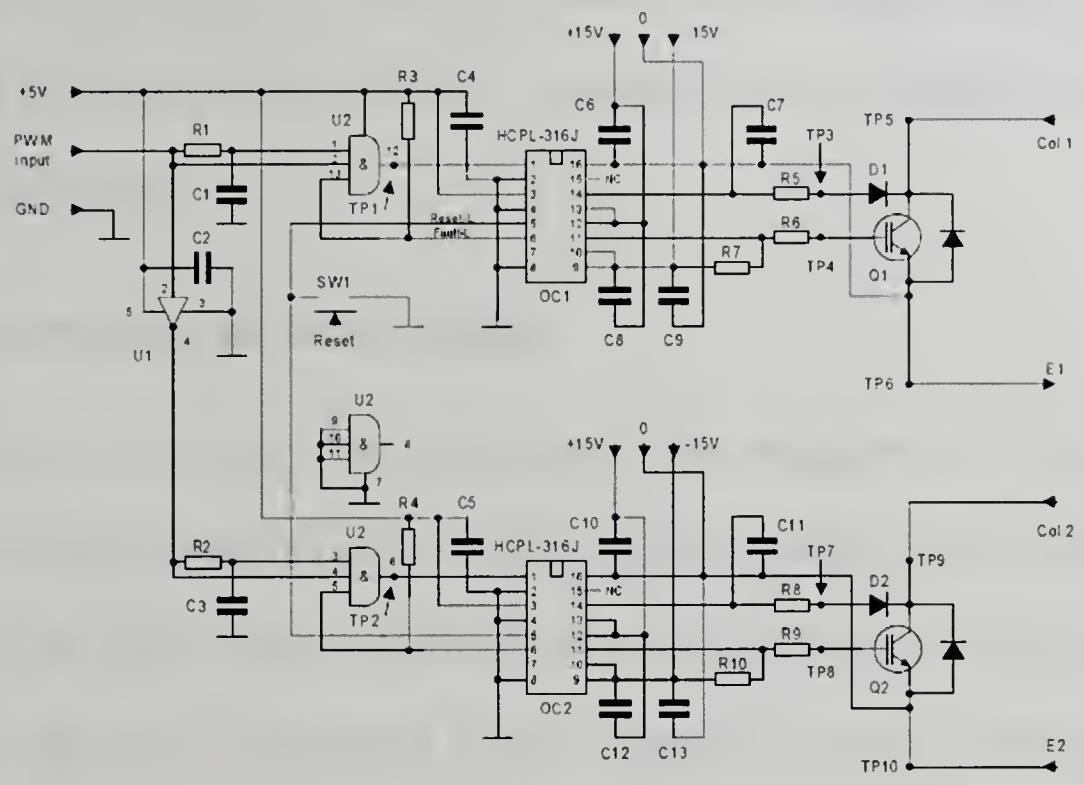


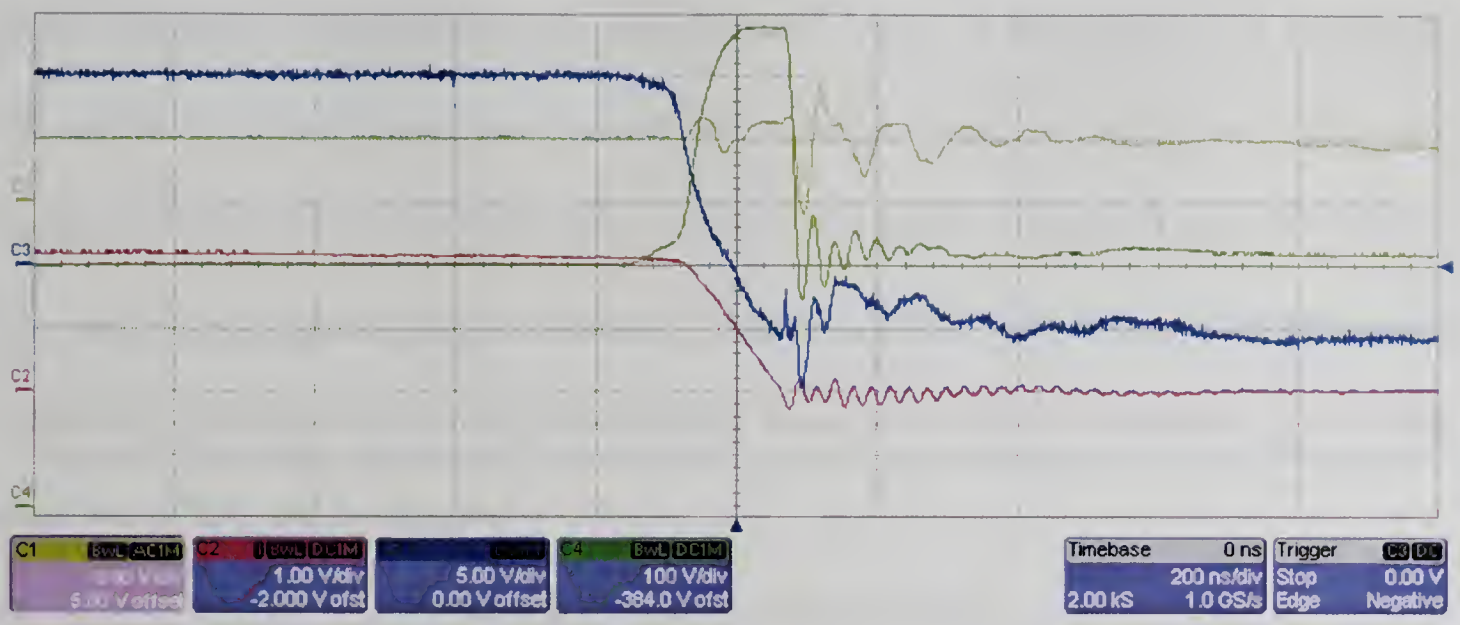
Figure 28: HCPL-316J evaluation board schematic [64]

8. OBSERVATIONS AND ANALYSIS

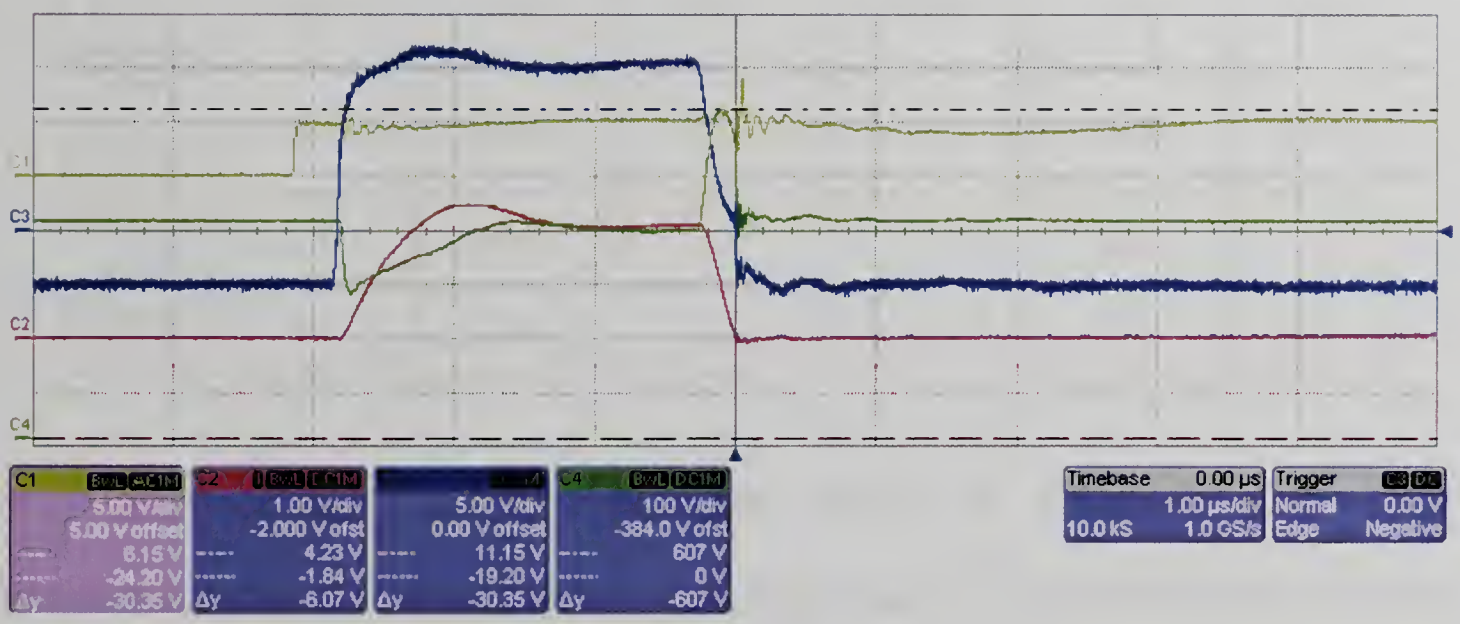
This chapter describes the behavior of IGBTs during each condition (overcurrent and short-circuit) and tabulates the observations of voltage overshoot difference and pulse energy difference during hard and soft turn-off. The first section of this chapter describes the waveforms and attributes of an example short-circuit test, as a prelude to discussion of experiments. Appendices B and C include the tables with detailed observations.

8.1. Description of an Example

Details of the set-up including circuitry are mentioned in Chapter 6. An example of a short-circuit test with the Infineon IKW30N60T IGBT is described in this section; see Figure 29(a) and (b). During the test, the input logic gate pulse (Channel 1), the current through the IGBT (Channel 2), the gate drive output pulse (Channel 3), and the collector-emitter voltage across the IGBT (Channel 4) were monitored. The test pulse was triggered across the gate-source terminals and the load was shorted. A drastic difference in overshoot voltage of the order of ~150 V (Channel 4) is observed. Details for all the tests and their results are tabulated in Appendices B and C. Also conspicuous in the waveforms is the desaturation detection and consequent turn-off of the gate output voltage even when the logic input is still on. Typical results for the IGBTs showed that while the hard turn-off time was ~500 ns maximum, soft turn-off reached ~1 μs, almost double that time in many occasions; i.e., the duration of the turn-off was increased by twice during soft turn-off in many cases.



(a)



(b)

Figure 29: Comparing gate voltages, collector current, and collector-emitter voltage during (a) hard turn-off and (b) soft turn-off of IKW30N60T IGBT; the time-scale for the (a) waveforms is 500 ns whereas that of the (b) set of waveforms is 1 µs; the vertical scales are equal

8.2. Overcurrent Scenario

Soft turn-off in overcurrent situations implied more energy being used by the pulse. Hence, there is a reduction in turn-off voltage overshoot but increase in overall energy dissipation. This is directly equivalent to the energy dissipated by the device during the pulse switching. Table 3 shows overcurrent test results for the different

IGBT structures. The difference in overshoot in Table 3 is between that of hard turn-off and soft turn-off since the former had a larger value for the same. The pulse energy difference is the excess energy used by the pulse during soft turn-off. This is for just one switching pulse: manually triggered. Since overcurrent conditions are relatively rare, the manual trigger instead of a continuous duty ratio input gives a fair estimate of the real conditions.

Table 3: Overcurrent analysis results

IGBT Type	Hard Turn-off Overshoot	Soft Turn-off Overshoot	Difference In Overshoot voltage (V)	Energy During Hard Turn-off (mJ)	Energy During Soft Turn-off (mJ)	Pulse Energy Difference (mJ)
FS Trench (Infineon)	467	428	39	39.4	47.1	7.4
NPT Planar (Infineon)	415	390	25	32.1	47.5	15.4
PT Planar (IR)	421	407	14	54.6	60.5	5.9
PTTrench (IR)	750	648	102	18.7	25.1	6.4

It was observed that overvoltages across the PT-trench IGBT from International Rectifier during turn-off were higher than any other IGBTs. Even during soft turn-off the absolute value of the overvoltage was very high, in spite of the reduction. Also, the difference in overvoltage was the highest in the PT-trench IGBT, with among the least increase in pulse energy (6.4 mJ). The PT-planar IGBT showed the least increase in pulse energy but also the least overvoltage decrease. Overall, the trench IGBTs showed greater decrease in overshoot voltage than their planar counterparts.

8.3. Short-Circuit Scenario

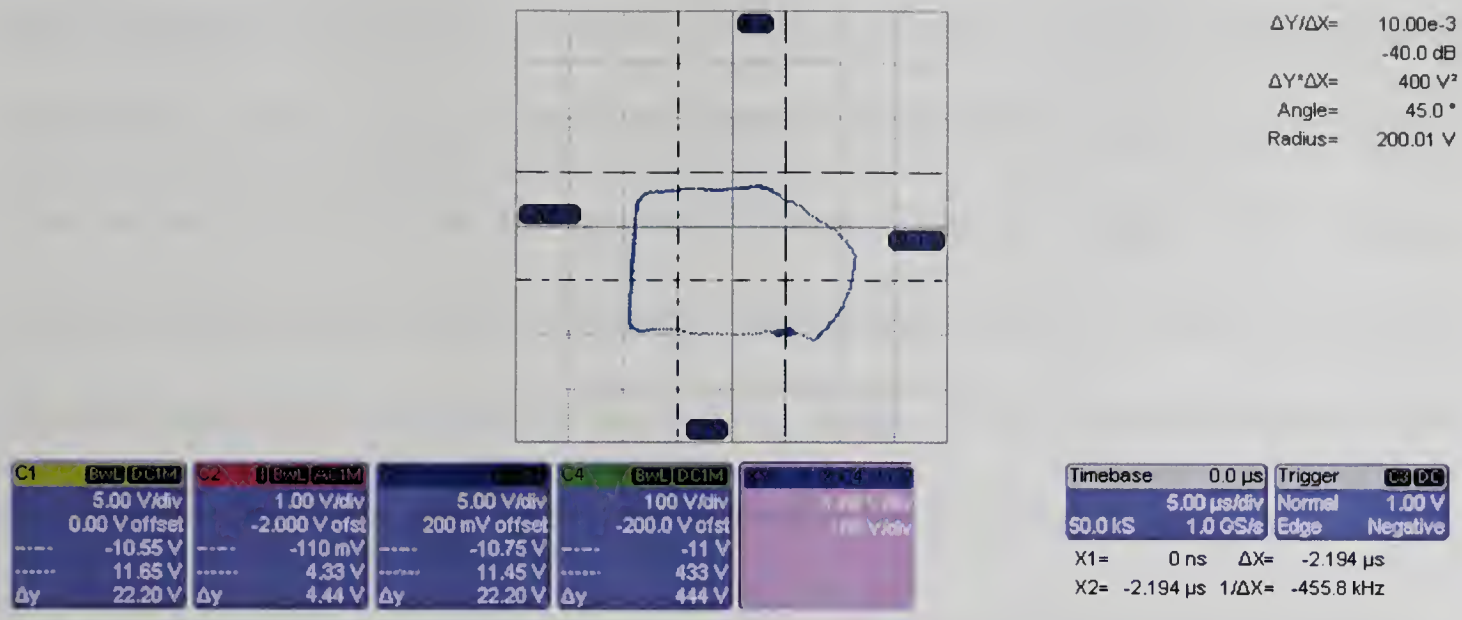
Table 4 shows that soft turn-off reduces not only the overshoot voltage but also the total energy under the pulse. Owing to short-circuit condition across the device, the current waveform is very similar in both scenarios. The difference in overshoot was more than 100 V in the trench IGBT cases, proving that soft turn-off was needed for trench IGBTs.

Table 4: Short-circuit analysis results

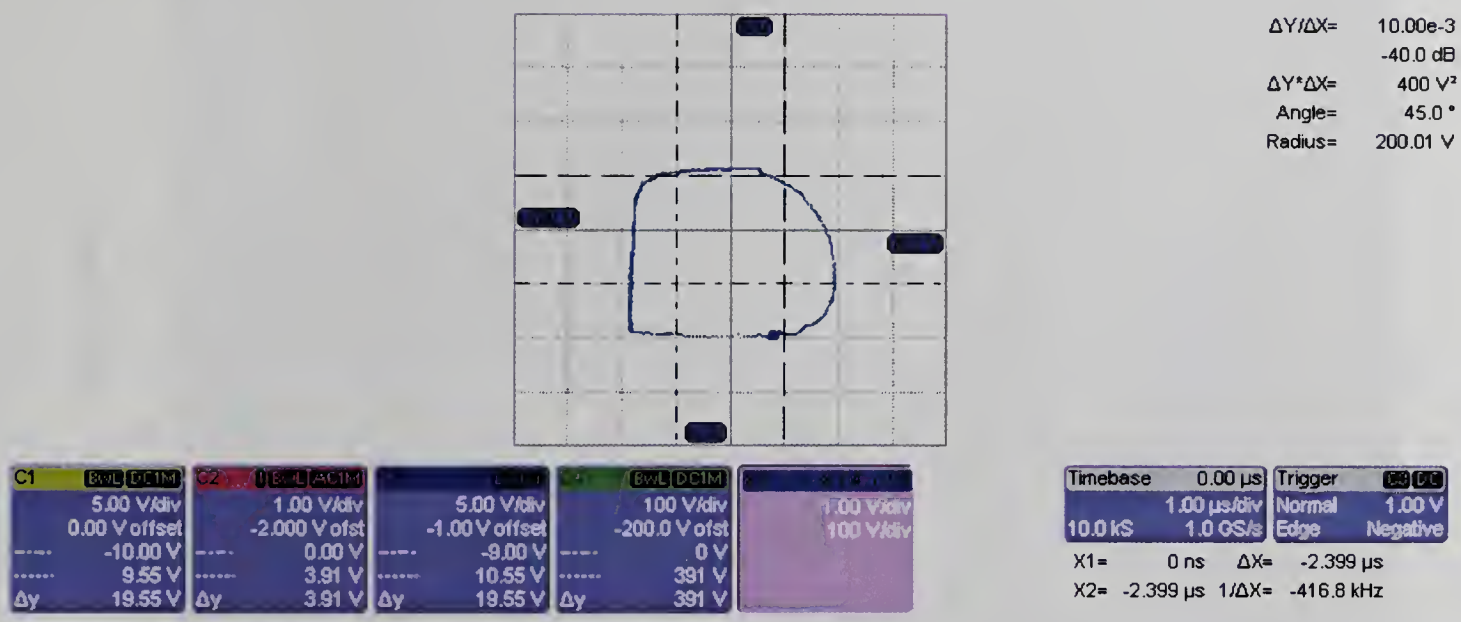
IGBT Type	Overshoot Difference (V)	Hard Turn-off Overshoot	Soft Turn-off Overshoot	Pulse Energy Reduction (mJ)	Energy During Hard Turn-off (mJ)	Energy During Soft Turn-off (mJ)
FS Trench (Infineon)	155	763	608	2.6	22.1	19.4
NPT Planar (Infineon)	35.8	854	711	3	22.6	19.6
PT Planar (IR)	101	706	605	14.6	38.7	24.1
PT Trench (IR)	158	785	627	3.4	17.5	14.1

An alternate method of analyzing the above data is to examine the switching trajectories of the devices. Typically, the safe operating area will be violated, especially in the short-circuit case. However, the single manual pulse, in most cases, does not cause device rupture. Rather, it enables a snapshot view of the typical expectations when the envelope of device tolerance is pushed.

Figure 30 shows an example of the planar NPT IGBTs' switching trajectories and a comparison between them. In the oscilloscope waveforms, the horizontal axis ranges from -200 to 600 V (100 V/div), whereas the vertical axis ranges from -200 to 600 A.



(a)



(b)

Figure 30: Overcurrent switching trajectories of the planar NPT IGBT (a) hard turn-off and (b) soft turn-off

The area within the trajectory gives an idea of power dissipated and the extent of the current (*y*-axis) and voltage (*x*-axis) reached during the switching period provides a thought on the extent of stress on the device. The current viewing shunts used were 10 mΩ as mentioned earlier. Hence, dividing the voltage on the *y*-axis by 10 mΩ gives a fairly accurate estimate of the current. As is evident from Figure 30, the soft turn-off trajectory shows an overall larger area but less stress on the voltage

axis. The hard turn-off results in higher overshoot voltage, hence the graph protrudes towards the positive *x*-axis (towards the right). Comparatively, the soft turn-off graph does not exceed 400 V on the horizontal direction but goes higher in the vertical direction, indicating a longer switching time but less overshoot. Ideally, the device trajectory should be less than the breakdown voltage in the horizontal direction and less than or equal to its rated continuous current in the vertical direction.

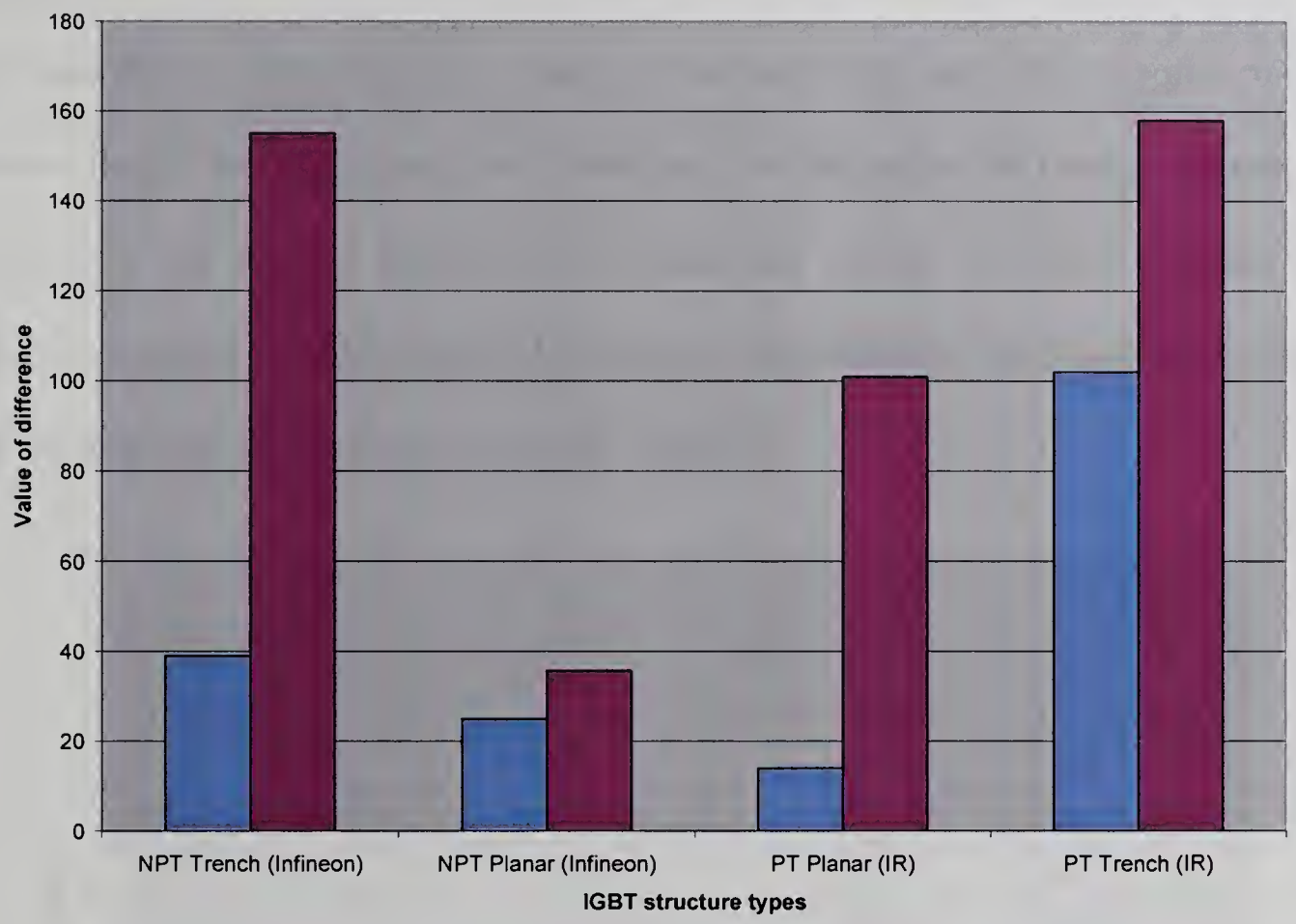


Figure 31: Quantified results of voltage overshoot difference: overcurrent (light column) and short-circuit (dark column) test results for each IGBT type shown

It is further observed from Appendices B and C that current levels higher than SOA limits discussed in Section 4.4 have consistently been reached during both overcurrent and short-circuit tests. The devices, however, did not rupture since the protection circuitry was enabled and shut them down within 2-3 μs. This further enhances that the short-circuit current limits provided by the manufacturer are

conservative.

8.4. Quantification of Test Data

The bar charts in Figures 31 and 32 quantify the observations that have been made during the tests. Figure 31 shows the difference in overshoot incurred by each IGBT type during overcurrent and short-circuit testing. Figure 32 shows the difference in pulse during energy overcurrent and short-circuit tests. The energy pulse difference during overcurrent tests equals the excess energy used during soft turn-off, whereas that of the short-circuit test describes the reduced pulse energy. Ideally, in overcurrent, soft turn-off should lead to maximum voltage overshoot decrease but minimum increase in pulse energy. In short-circuit, ideally the maximum decrease in both pulse energy and voltage overshoot is desired.

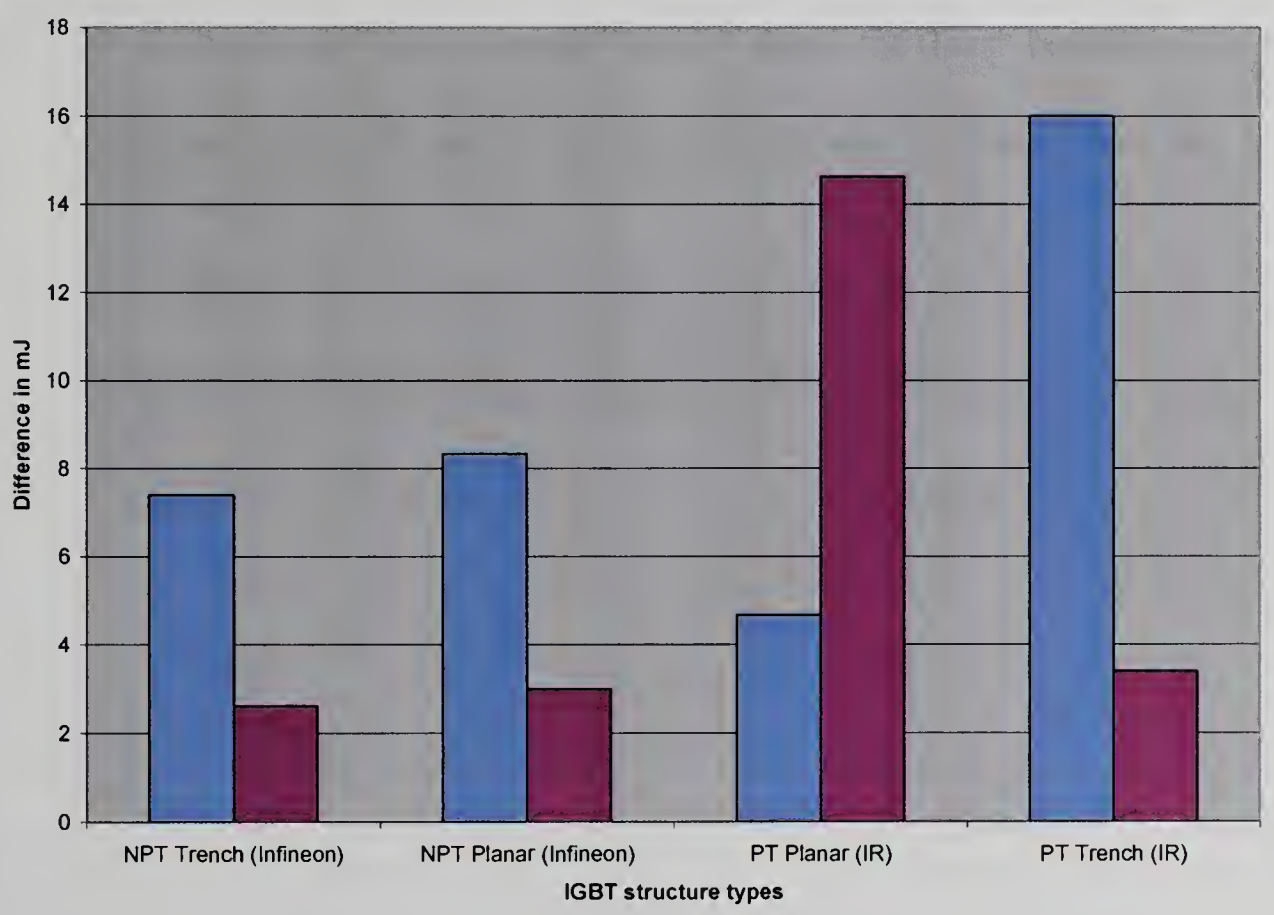


Figure 32: Quantified results of pulse energy difference: overcurrent (light column) and short-circuit (dark column) test results for each IGBT type shown

During short-circuit tests, soft turn-off greatly reduces overshoot voltage, as evident in Figure 31. The energy reduction during short-circuit is insignificant (except in the punch-through planar IGBT), because the current and voltage values are high for most of the on-state situation, until the detection and turn-off is expected. The huge reduction of voltage overshoot in both cases is expected. However, during overcurrent conditions, the excess pulse energy used is high (except for the punch-through planar IGBT). The NPT planar IGBT gives the least reduction in overshoot voltage at a considerable increase in pulse energy. Hence, should a trade-off scenario arise, the NPT planar IGBT would be the first target, as far as steering away from the added cost of soft turn-off is concerned.

As has been seen in Figures 31 and 32, the trench IGBTs show the greatest difference in overshoot voltage reduction in both overcurrent and short-circuit cases. However, in short-circuit cases, trench IGBTs show the least reduction in pulse energy. Hence, soft turn-off needs to be used for applications involving trench IGBTs.

9. CONCLUSIONS AND FUTURE WORK

9.1. Conclusions

Soft turn-off reduces overvoltage stress on a device, enabling higher reliability as far as collector-emitter breakdown voltage is concerned. The rule-of-thumb of operating bus voltage to be 80% of the device breakdown rating has been assumed. Energy dissipation during soft turn-off remains a trade-off, not only in terms of power loss but also in terms of dissipation having the potential to hurt the device. This is keeping in mind the strong possibility of a temporary overcurrent, thereby expecting the device to resume normal operation.

As far as short-circuit protection goes, soft turn-off should definitely be incorporated, owing to the immediate need to turn off the device and reduce the chances of type II rupture. This is proved in Chapter 7 and is shown by both the tabular representation of data and the bar charts. The bar charts show huge improvement in overshoot voltage, with little increase in overall pulse area. Also, chances of immediate operation resumption are rare since the gate drive will require a reset for the same to occur. The high current during this condition, if turned off rapidly, could induce enough overvoltage to destroy the device. Losses then should not be a concern.

During overcurrent conditions, the increase in pulse energy is important. No structure except the punch-through trench IGBT shows significant decrease in overshoot voltage by incorporation of soft turn-off. However, the pulse energy used is higher, when compared to the decrease in overvoltage. Hence, there is a risk of device

rupture due to internal heating, caused by delayed turn-off. There is no linear relationship between the amount of overvoltage reduced by hard turn-off and the change in pulse energy, in either case. A quantitative observation based on validation has been arrived at, and the detailed data have been included in Appendices B and C.

9.2. *Future Work*

It is recommended that trench IGBT applications also incorporate soft turn-off for short-circuit applications. Smaller area and overall thinner structure of trench technology could mean better power dissipation out of the device. However, by easily dissipating heat, overvoltage breakdown is not ruled out. In other words, the power may be dissipated easily, but the breakdown voltage tolerance may not be and most likely is not favorable due to the structure.

Secondly, it is also recommended that a gate driver be designed to recognize the current level in the device and decide whether hard or soft turn-off should be incorporated should a fault arise. For this functionality to be integrated, knowledge of the collector voltage, along with extent of current and instantaneous power being dissipated, is necessary. The two-step logic would decide if a turn-off is necessary, and what kind of turn-off is optimal given the instantaneous values of the collector-emitter current, voltage, and power being dissipated.

APPENDIX A: SCHEMATIC OF HARDWARE VALIDATION LAYOUT

Figure 33 shows the schematic of the Infineon driver set-up to test hard turn-off situations of the IGBTs. The drive-side circuitry, the IGBT under test, current viewing resistor, and the current transformer are shown. Included in the details of the gate drive circuitry is the desaturation detecting diode D1 connected between pin-2 of the driver chip and the collector of the IGBT. This diode is in series with a time defining resistor-capacitor network. This decides the dormant time of the destaturation detection circuit. The circuit needs to be inactive about 2-3 μs after turn-on to allow the noise related oscillations to settle, before fault detection can be initiated. This avoids parasitic turn-off due to incorrect fault detection. The zener capacitor parallel network out of pin-4 was initially supposed to define the voltage level and timing for the two-level turn-off, to reduce overvoltage. However, the driver chip did not come with that functionality; it was scheduled to be incorporated and released after the time allotted for test validation had passed.

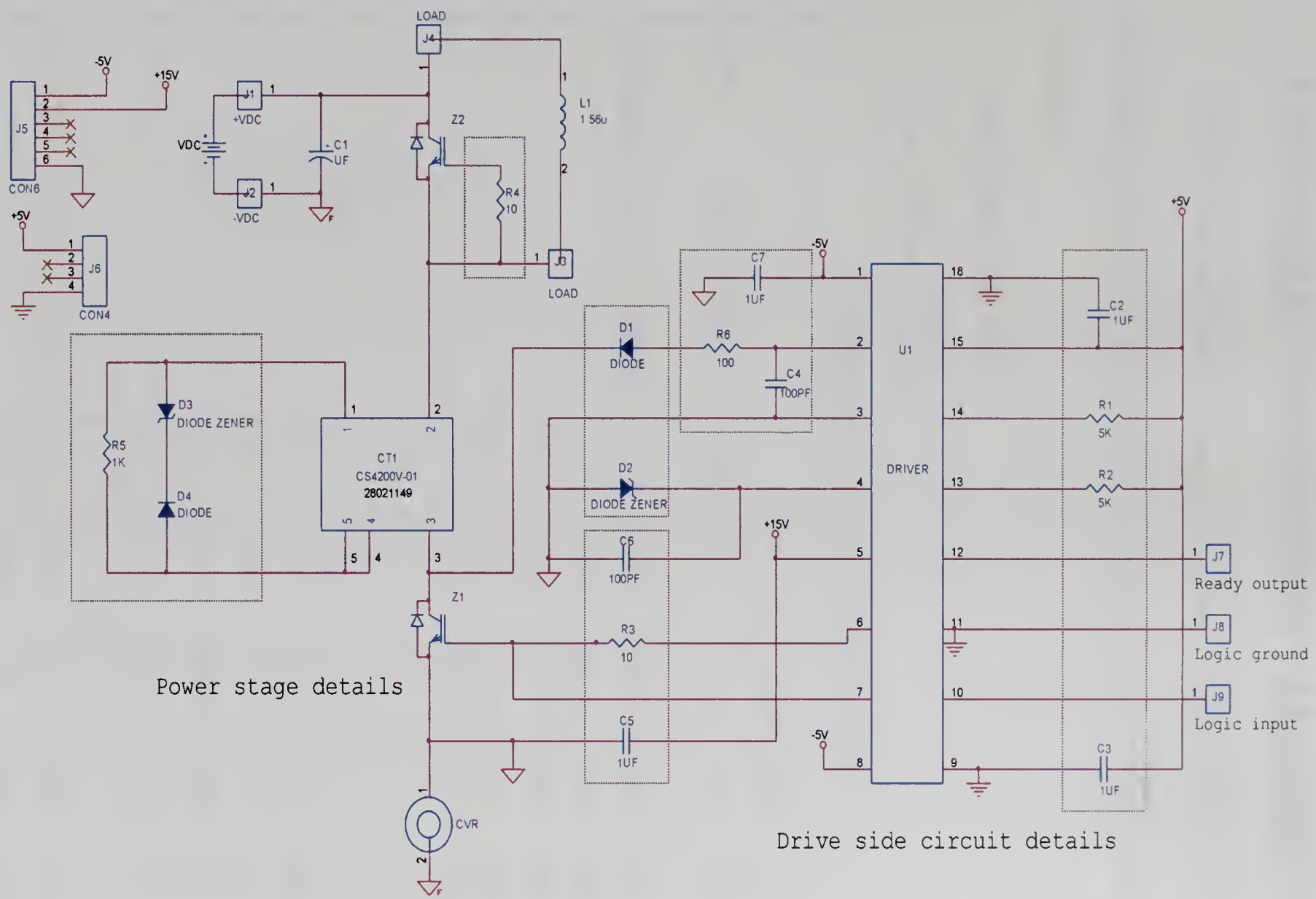


Figure 33: Schematic of Infineon driver setup

APPENDIX B: OVERCURRENT ANALYSIS DATA

Table 5 lists the results of overcurrent tests on the different IGBT structures. Assuming everything else in the setup is constant, the test conditions have been stated as follows:

- Bus voltage: 100-300 V.
- Load inductor: 1.56 μH.

Table 5: Overcurrent analysis observations

IGBT	Driver	Type	Output	DC Vol. (V)	Current (A)	Ovsht (V)	% Ovsht	Energy (Scaled) mJ
SKW30N60HS	Infineon	Planar NPT	4.8	100	235	302	202	4.43862
			4	150	259	335	123.333	7.792
			2.9	200	269	337	68.5	28.4
			2.5	250	262	403	61.2	19.329
			2.2	300	273	415	38.3333	32.062
	Avago		4.5	100	212	197	97	8.986
			4	150	296	256	70.6667	19.8
			3.5	200	317	305	52.5	28.3
			2.8	250	311	342	36.8	38.6
			2.4	300	311	390	30	47.5
IKW30N60T	Avago	FS Trench	4.8	100	246	234	134	10.9304
			3.9	150	293	287	91.3333	19.944
			3	200	296	339	69.5	27.71
			2.4	250	285	380	52	32.451
			2.1	300	282	428	42.6667	47.128
	Infineon		4.7	100	235	306	206	8.217
			3.3	150	245	330	120	15.86

Table 5 (continued)

IGBT	Driver	Type	Output	DC Vol. (V)	Current (A)	Ovsht (V)	% Ovsht	Energy (Scaled) mJ
			2.6	200	245	360	80	22.096
			2.2	250	247	415	66	29.8
			1.95	300	247	467	55.6667	39.696
IRGPC50UD2	Infineon	PT Planar	7.2	100	349	278	178	7.37
			4.8	150	364	323	115.333	15.969
			3.8	200	385	350	75	23.797
			3.17	250	395	398	59.2	37.765
			2.75	300	395	421	40.3333	54.596
	Avago		5	100	265	202	102	8.294
			4.56	150	351	258	72	22.736
			4	200	414	312	56	36
			3.4	250	427	357	42.8	49.1
			2.8	300	411	407	35.6667	60.5
IRGP4062D	Avago	PT Trench	4	100	186	530	430	7.96
			3.4	150	218	508	238.667	8.7
			2.6	200	221	558	179	17.6
			2.3	250	226	604	141.6	23.25
			2	300	228	648	116	25.1
	Infineon		3.65	100	163	690	590	6.195
			2.5	150	169	680	353.333	9.093
			2.1	200	169	700	250	16.12
			1.79	250	173	730	192	17.05
			1.53	300	173	750	150	18.7

APPENDIX C: SHORT-CIRCUIT ANALYSIS DATA

Table 6 lists the results of short-circuit tests on the different IGBT structures. The test conditions have been stated as follows:

- No load inductor was included.
- Bus voltage: 400 V.

Table 6: Short-circuit analysis observations

IGBT		Output PW (uSec)	Current (A)	Ovsht (V)	% Ovsht	Energy (Scaled)
IRGPC50UD2						
	Infineon driver	3.15	371	706	76.5	38.73
	Turn-off Observations:					
	Current to 0: 386 ns					
	Gate Voltage 15 to -5: 142 ns					
	Avago Driver	3	245	605	51.25	24.1
	Turn-off Observations:					
	Current to 0: 360 ns					
	Gate Voltage 15 to -5: 238 ns					
	followed by spike and then total					
	of 600 ns turn-off					
IKW30N60T						
	Avago Driver	2.8	246	608	52	22.09
	Turn-off Observations:					
	Current to 0: 245 ns					
	Gate Voltage 15 to -5: 290 ns					
	Clearly shows soft turn-off					

Table 6 (continued)

IGBT		Output PW (uSec)	Current (A)	Ovsht (V)	% Ovsht	Energy (Scaled)
	Infineon driver	2.6	227	763	90.75	19.47
	Turn-off Observations:					
	Current to 0: 132 ns					
	Gate Voltage 15 to -5: 196 ns					
SKW30N60HS	Avago Driver	2.7	225	711	77.75	22.6
	Turn-off Observations:					
	Current to 0: 205 ns					
	Gate Voltage 15 to -5: 420					
	Infineon driver	2.4	253	854	113.5	19.6
	Turn-off Observations:					
	Current to 0: 150					
	Gate Voltage 15 to -5: 280					
IRGP4062D	Avago Driver	3	170	627	56.75	17.5
	Turn-off Observations:					
	Current to 0: 200					
	Gate Voltage 15 to -5: 430					
	Infineon driver	2.3	186	785	96.25	14.1
	Turn-off Observations:					
	Current to 0: 145					
	Gate Voltage 15 to -5: 160					

APPENDIX D: EQUIPMENT USED FOR HARDWARE VALIDATION

Table 7 shows the list of the equipment used for hardware validation. The respective manufacturer's web site may be accessed for more information.

Table 7: List of equipment

Equipment Type	*Manufacturer and Model Number*
Oscilloscope	Lecroy Wavesurfer 424 200 MHz Scope
Gate Drive Power Supplies	Tektronix Laboratory DC power supply PS280
Power Stage DC Supply	HP Cap Bank high power supply 6035A
Arbitary Waveform Generator	Arbitary/ Function Generator Tektronix AFG3102
Multimeter	Fluke 8062A True RMS Multimeter

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7/16/2008
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